2ch Digital isolator

Isolation voltage 2500 Vrms High Speed Isolator

BM67220FV-C

●Description

The BM67220FV-C is a high-speed isolator IC used in electric vehicles and hybrid vehicles. This IC features dielectric strength of 2500 Vrms between I/O and the maximum propagation delay time of 45ns.

●Features

1) Dielectric strength of 2500 Vrms between I/O
2) Maximum propagation delay time of 45 ns
3) Built-in 2ch uni-directional propagation

●Applications

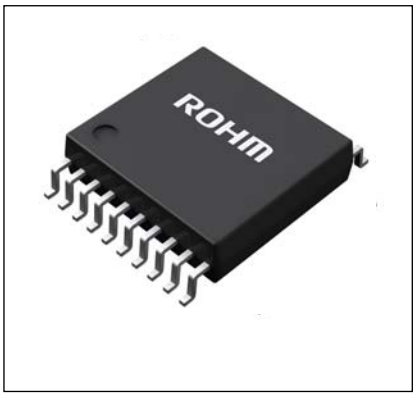
Propagation of logic signal within electric and hybrid vehicles

●Key Specification

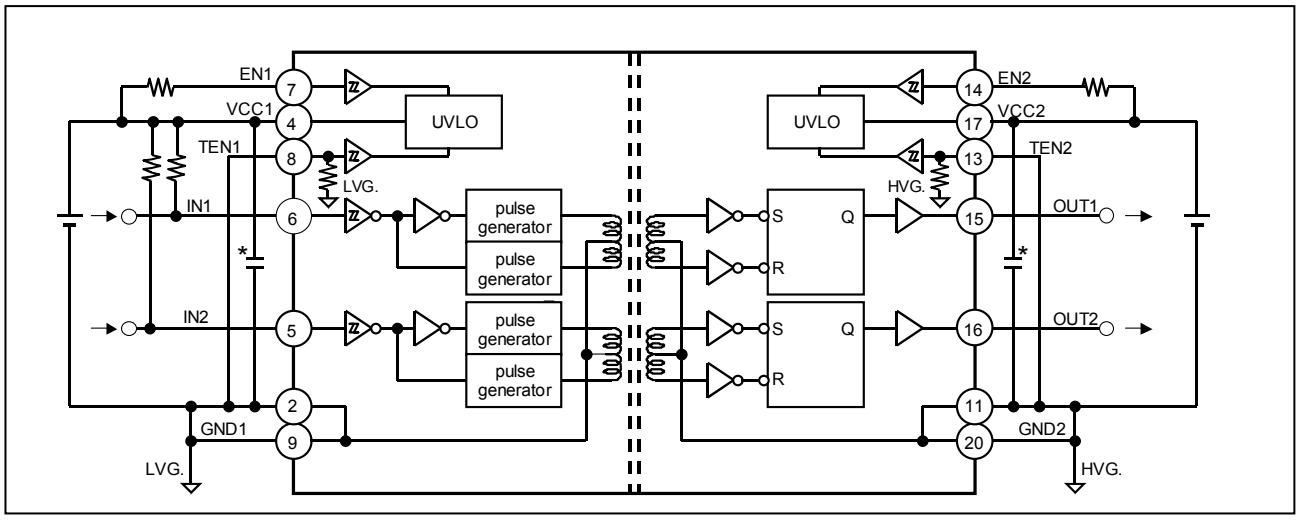
- Supply voltage range: 4.5V to 5.5V
- Propagation delay: 45ns(Max.)
- Stand-by Current: 0μA (Typ.)
- Operating temperature range: -40℃ to 125℃

●Package

	W(Typ.) x D(Typ.) x H(Max.)
SSOP-B20W	6.50mm x 8.10mm x 2.01mm



●Typical Application Circuit



* Please connect bypass capacitor directly to the IC's pin.

Figure 1. BM67220FV-C Application examples

●**Pin Configuration**

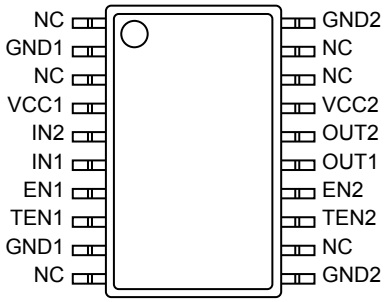


Figure 2. BM67220FV-C Package (SSOP-B20W)

●**Pin Description**

No.	Pin Name	Function	No.	Pin Name	Function
1	NC	Non Connect	20	GND2	Ground
2	GND1	Ground	19	NC	Non Connect
3	NC	Non Connect	18	NC	Non Connect
4	VCC1	Power supply	17	VCC2	Power supply
5	IN2	Input 2	16	OUT2	Output 2
6	IN1	Input 1	15	OUT1	Output 1
7	EN1	Enable input	14	EN2	Enable input
8	TEN1	Test mode input	13	TEN2	Test mode input
9	GND1	Ground	12	NC	Non Connect
10	NC	Non Connect	11	GND2	Ground

●Description of Operation

1)Input/Output logic

The input/output logic levels for the BM67220FV-C are as shown in the table below.

No.	EN1	EN2	IN1	IN2	OUT1	OUT2
1	L	L	X	X	L	L
2	L	H	L	L	*	*
3			L	H	*	*
4			H	L	*	*
5			H	H	*	*
6	H	L	L	L	L	L
7			L	H	L	L
8			H	L	L	L
9			H	H	L	L
10	H	H	L	L	L	L
11			L	H	L	H
12			H	L	H	L
13			H	H	H	H

* Retains its previous state

If the EN1 and EN2 pin is set to the “L” (Low) logic level, the OUT1 and OUT2 pin will be set to the “L” logic level.
If the EN1 pin is set to the “L” logic level and the EN2 pin is set to “H” logic level, the OUT1 and OUT2 pins will be retained its previous state.
If the EN1 pin is set to the “H” logic level and the EN2 pin is set to “L” logic level, the OUT1 and OUT2 pins will be set to “L” logic level.
If the EN1 and EN2 pins are set to the “H” logic level, the output logic level of the OUT1(OUT2) pin will vary with the input logic level of the IN1(IN2) pin.
Furthermore, no pull-up/pull-down resistor is connected to the IN1, IN2, EN1, and EN2 pins. Consequently, in order to fix the input logic levels of the IN1, IN2, EN1, and EN2 pins, external resistor should be connected to the relevant pin, respectively.

2) TEN pins

The TEN pins serve as a test enable pin, respectively.
Please connect to GND. If you do not connect to GND ,there is possibility of malfunction.

3) Output pin voltage

Logic levels for output pins come to those listed in the truth value table in Sections 1), 6), and 7). However, it may be assumed that such logic levels disable the output circuit to fully turn ON at a low voltage when turning ON or OFF the power supply, thus putting the output pin into the high impedance state.

4) Under voltage lock out

If the VCC2≧4.0 (typ.) and the VCC1 pin voltage falls below 3.8V(typ.), the OUT1 and the OUT2 pins will be retained its previous state.
If the VCC1 24.0V(typ.) and the VCC2 pin voltage falls below 3.8V(typ.), the OUT1 and the OUT2 pins will be set to the “L” logic level.
If the VCC1 and the VCC2 pins voltage fall below 3.8V(typ.), the OUT1 and the OUT2 pins will be set to the “L” logic level.
If the VCC1≧4.0V(typ.) and VCC2≧4.0V(typ.) , the output logic level of OUT1(OUT2) pin will vary with the input logic level of the IN1(IN2) pin.

5) Under Voltage Lock Out (UVLO) function masking time

This IC provides masking time for the UVLO function. The masking time is set to 10 μsec (Typ.).

6) Input/Output logic levels with power supply turned OFF
The following table shows output logic levels according to the order in which the power supply turns OFF.

No.	Power Supply	IN1	IN2	OUT1	OUT2
1	VCC1	L	L	L	L
2		L	H	L	H
3		H	L	H	L
4		H	H	H	H
5	VCC2	L	L	L	L
6		L	H	L	L
7		H	L	L	L
8		H	H	L	L

OUT1 logic level is changed to “L” and OUT2 logic level is changed to “L” when VCC2 power down.

7) Output logic levels with power supply turned ON
The following table shows output logic levels according to the order in which the power supply turns ON.

No.	Turning-ON Order1	Turning-ON Order2	IN1	IN2	OUT1	OUT2
1	VCC1	VCC2	L	L	L	L
2			L	H	L	L*
3			H	L	L*	L
4			H	H	L*	L*
5	VCC2	VCC1	L	L	L	L
6			L	H	L	H
7			H	L	H	L
8			H	H	H	H

*Different input and output logic

If the power supplies on the transmission side VCC1 are turned ON first, a pulse to be propagated will be output before the circuit on the receiving side VCC2 turns ON.
As a result, the circuit on the receiving side cannot receive the pulse propagated and the relevant pin is not set to the output logic level corresponding to the input logic level (see No. 2, 3, 4).

●**Timing Chart**

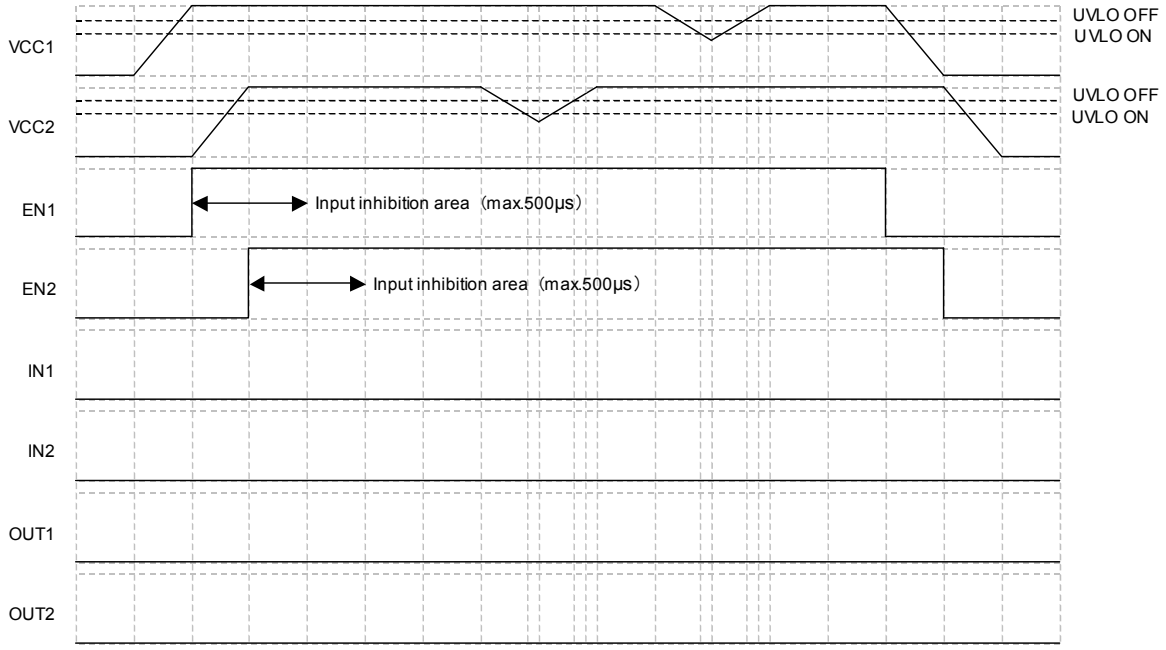


Figure 3. VCC1→VCC2（IN1=L, IN2=L）

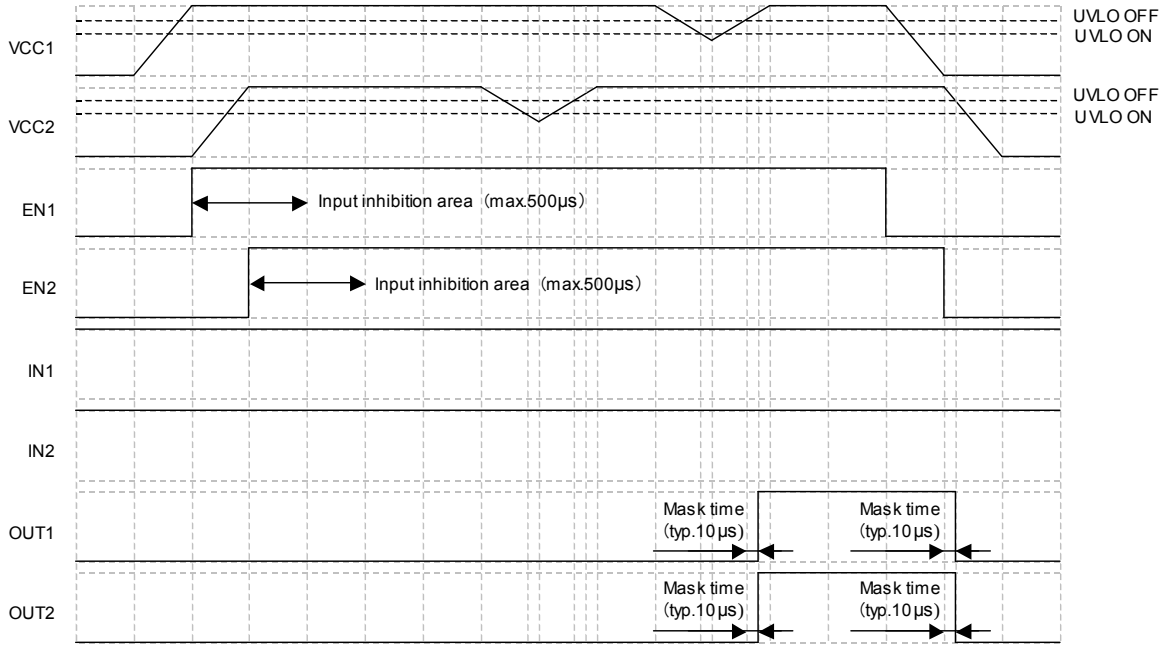


Figure 4. VCC1→VCC2（IN1=H, IN2=H）

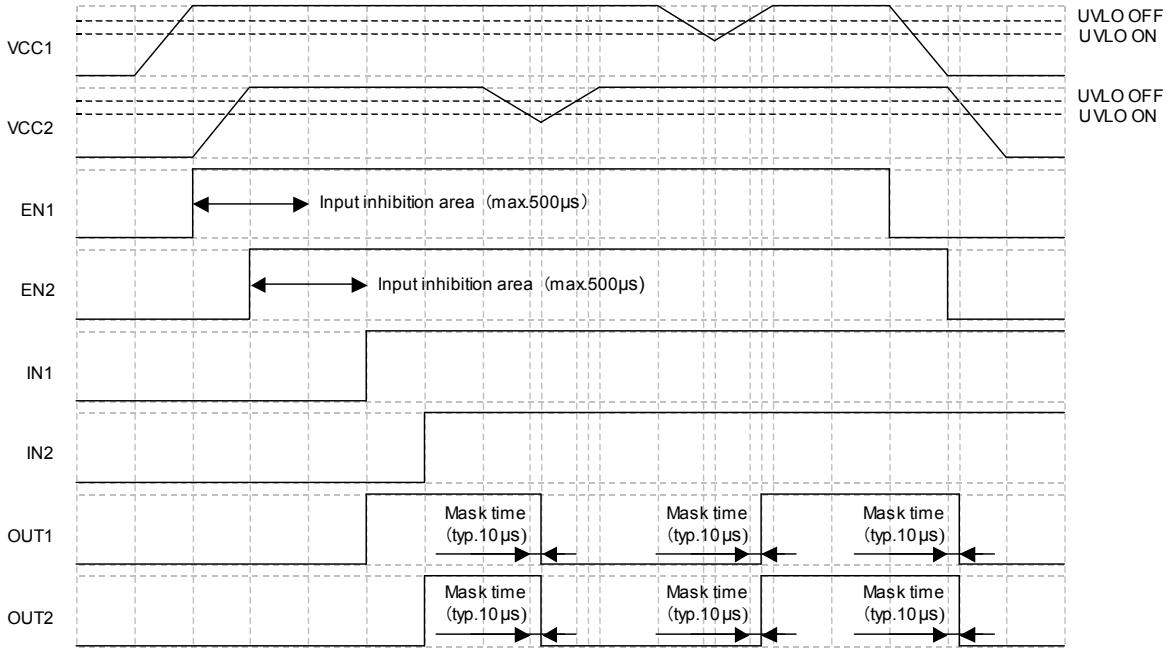


Figure 5. VCC1→VCC2（IN1=L→H, IN2=L→H）

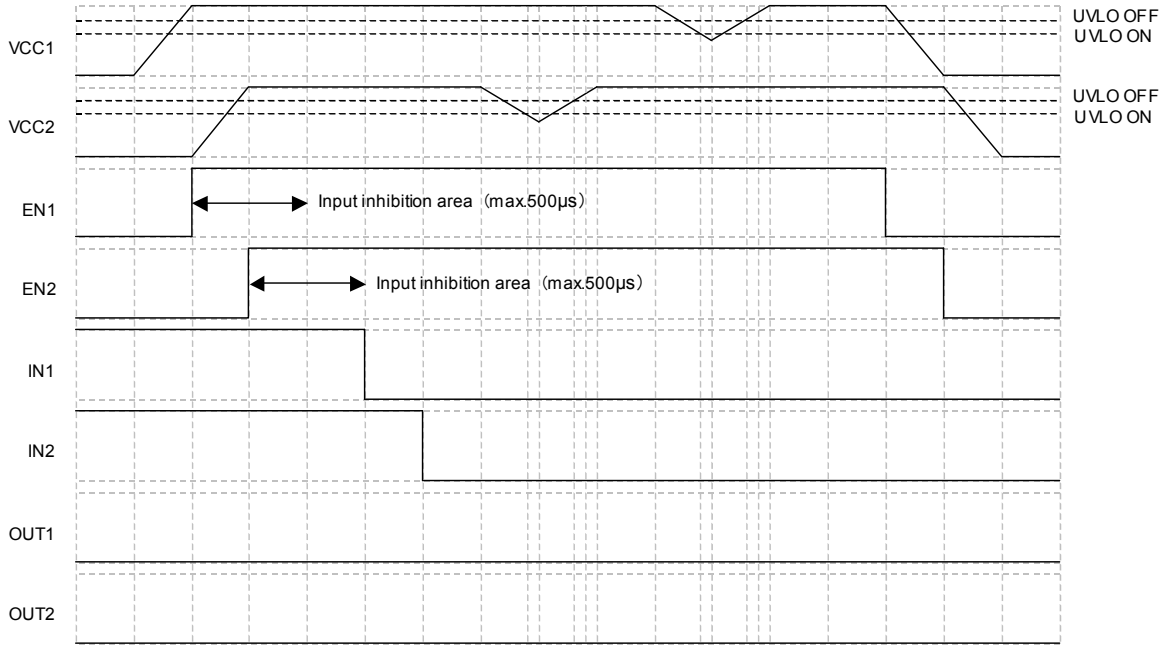


Figure 6. VCC1→VCC2（IN1=H→L, IN2=H→L）

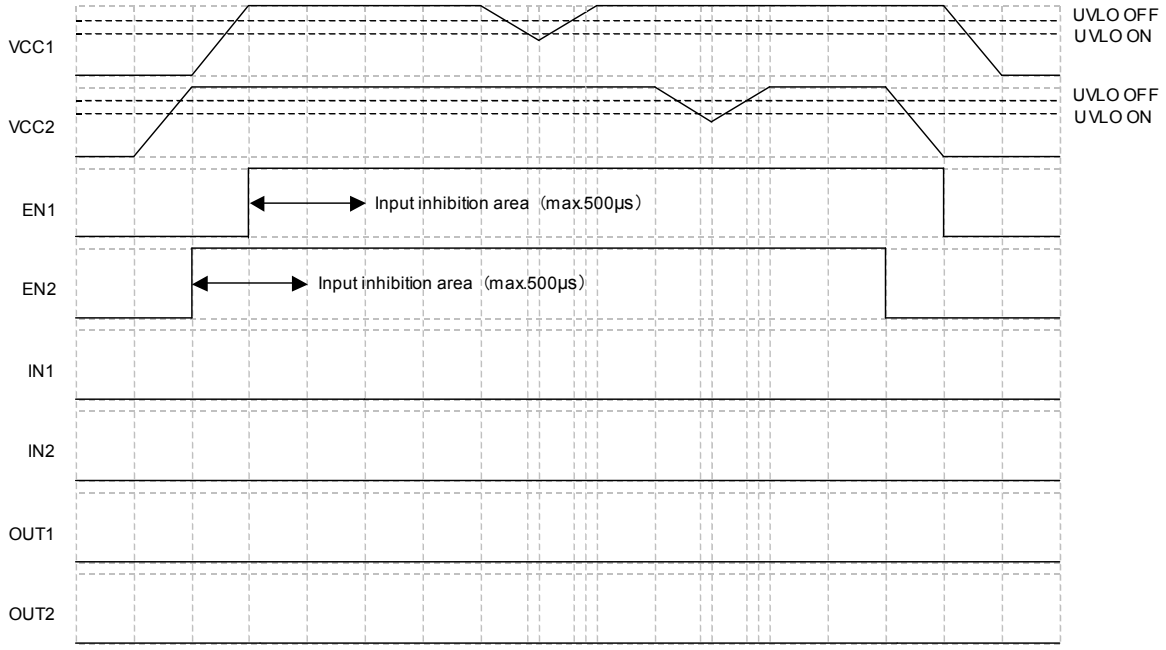


Figure 7. VCC2→VCC1（IN1=L, IN2=L）

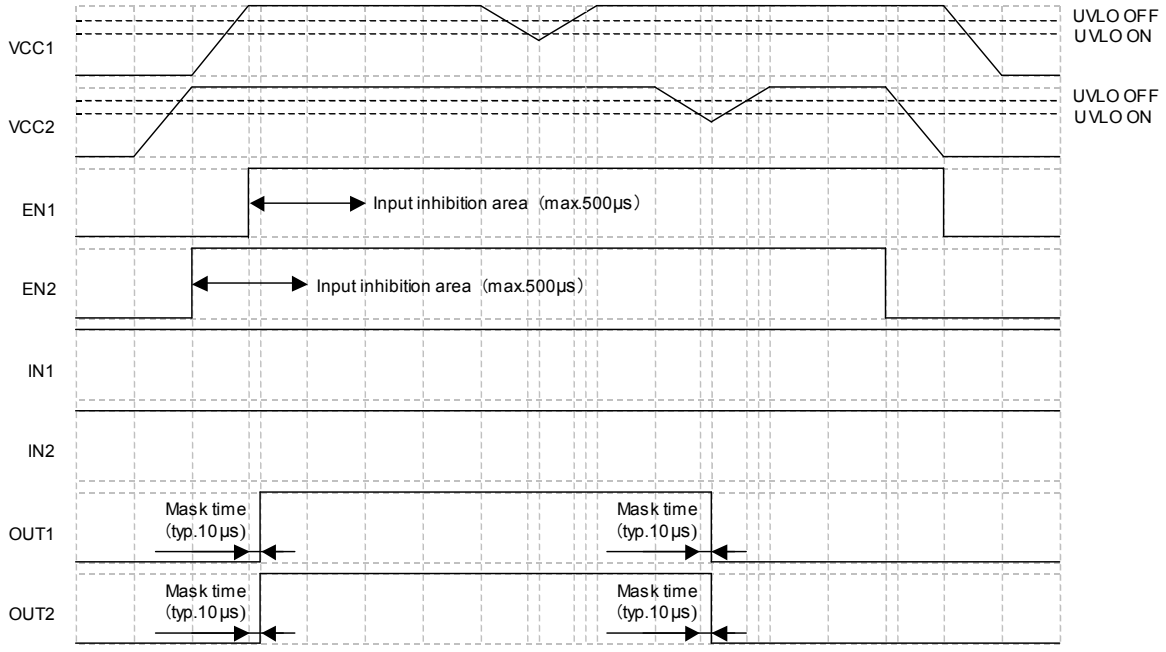


Figure 8. VCC2→VCC1（IN1=H, IN2=H）

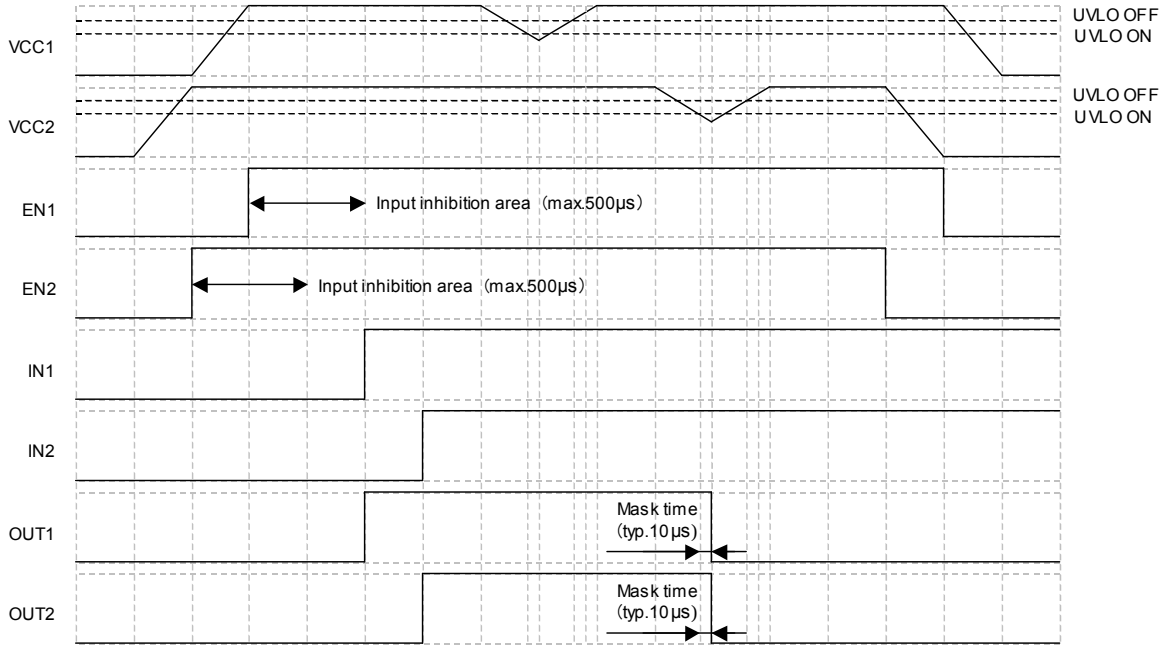


Figure 9. VCC2→VCC1（IN1=L→H, IN2=L→H）

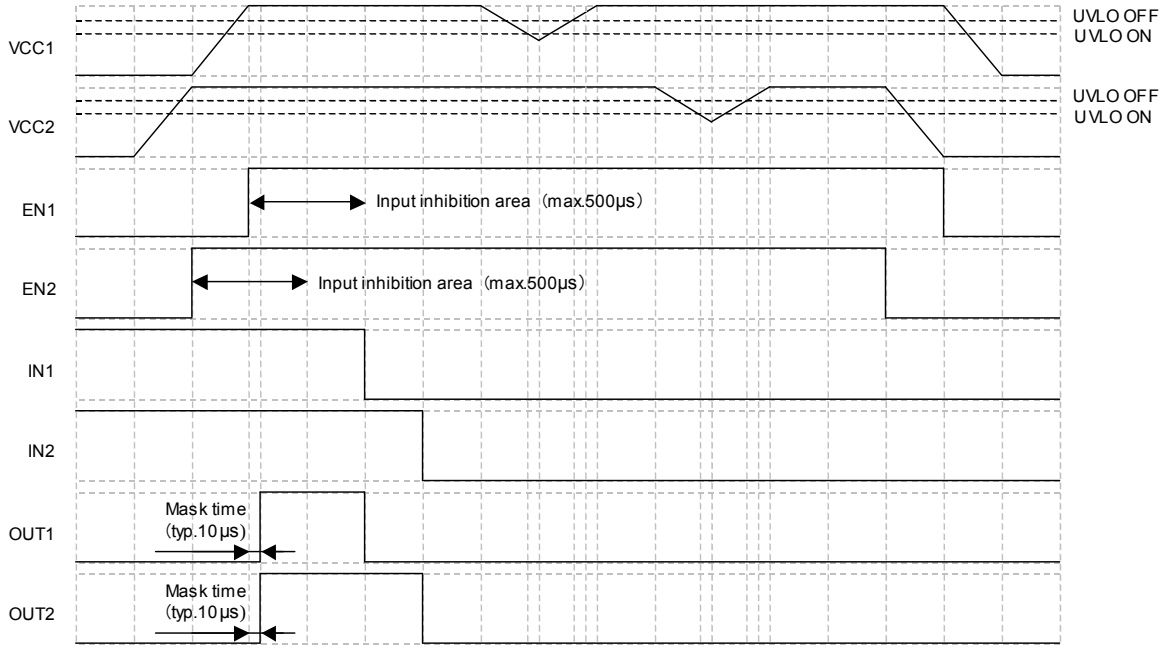


Figure 10. VCC2→VCC1（IN1=H→L, IN2=H→L）

●Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
		BM67220FV-C	
Power supply voltage 1	V_{CC1}	7.0*1	V
Power supply voltage 2	V_{CC2}	7.0*2	V
IN1 pin voltage	V_{IN1}	-0.3 ~ 7.0*1	V
IN2 pin voltage	V_{IN2}	-0.3 ~ 7.0*2	V
OUT1 pin voltage	V_{OUT1}	-0.3 ~ 7.0*2	V
OUT2 pin voltage	V_{OUT2}	-0.3 ~ 7.0*1	V
Output current	$I_{OMAX(OUT)}$	±10*3	mA
GND1-GND2 ground potential	V_{GND}	2500	Vrms
Operating temperature range	T_{OPR}	-40 ~ 125	°C
Storage temperature range	T_{STG}	-55 ~ 150	°C
Power dissipation	Pd	1.19*4	W
Maximum junction temperature	T_{jmax}	150	°C

*1 Based on GND1.
*2 Based on GND2.
*3 Should not exceed Pd and ASO.
*4 When mounted on a glass epoxy board measuring 70 mm × 70 mm × 1.6 mm (including a copper foil area of 3% or less).
To use the IC at Ta=25°C or higher, derate power rating by 9.52mW/°C.

●Operating Range

Parameter	Symbol	BM67220FV-C	Unit
Power supply voltage 1	V_{CC1}	4.5 ~ 5.5*5	V
Power supply voltage 2	V_{CC2}	4.5 ~ 5.5*6	V

*5 Relative to GND1
*6 Relative to GND2

●Insulation related characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance（V_{IO}=500V）	R_S	$>10^9$	Ω
Insulation Withstand Voltage/1min.	V_{ISO}	2500	Vrms
Insulation Test Voltage/1s	V_{ISO}	3000	Vrms

●**Electrical Characteristics (All values at Ta=-40°C ~125°C and VCC=4.5V~5.5V, unless otherwise specified)**

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
<Whole>						
VCC1 power supply current, quiescent	$I_{CC1STBY}$	-	0	10	μA	EN1 = 0
VCC2 power supply current, quiescent	$I_{CC2STBY}$	-	0	10	μA	EN2 = 0
VCC1 power supply current, DC	I_{CC1Q}	-	0.21	0.42	mA	V_{IN} = 0 or VCC
VCC2 power supply current, DC	I_{CC2Q}	-	0.21	0.42	mA	V_{IN} = 0 or VCC
VCC1 power supply current, 10kbps	I_{CC10k1}	-	0.23	0.50	mA	fin : 5kHz
VCC2 power supply current, 10kbps	I_{CC10k2}	-	0.22	0.48	mA	fin : 5kHz
VCC1 power supply current, 1Mbps	I_{CC1M1}	-	1.36	3.20	mA	fin : 500kHz
VCC2 power supply current, 1Mbps	I_{CC1M2}	-	0.40	1.00	mA	fin : 500kHz
IN1,IN2 Input inhibition area		-	-	500*7	μs	
<Output pin: OUT1 and OUT2>						
High-level output voltage	V_{OH}	V_{CC}-0.5	V_{CC}-0.3	V_{CC}	V	I_O=-5mA
Low-level output voltage	V_{OL}	0	0.2	0.4	V	I_O=5mA

*7Please do not switch the input signal IN1 and IN2 between Tin section. If there is a logic input and output does not match.

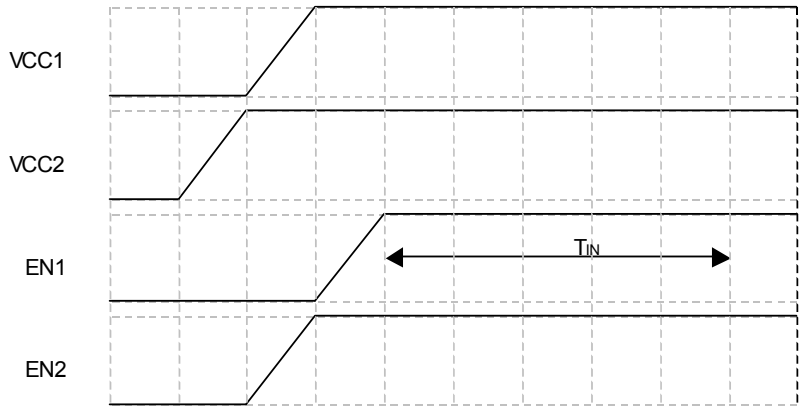


Figure 11. IN1,IN2 Input inhibition area

●**Electrical Characteristics (All values at Ta=-40°C ~125°C and VCC=4.5V~5.5V, unless otherwise specified)**

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
<Input pin: IN1 and IN2>						
Input current	I_{IN}	-	0	10	μA	V_{IN}=VCC
High-level input threshold	V_{INH}	V_{CC}×0.7	-	V_{CC}	V	
Low-level input threshold	V_{INL}	0	-	V_{CC}×0.3	V	
<Enable pin: EN1 and EN2>						
Input current	I_{EN}	-	0	10	μA	V_{EN}=VCC
High-level input threshold	V_{ENH}	V_{CC}×0.7	-	V_{CC}	V	
Low-level input threshold	V_{ENL}	0	-	V_{CC}×0.3	V	
<Test pin: TEN1 and TEN2>						
Input current	I_{TEN}	30	50	70	μA	V_{TEN}=VCC
High-level input threshold	V_{TENH}	V_{CC}×0.7	-	V_{CC}	V	
Low-level input threshold	V_{TENL}	0	-	V_{CC}×0.3	V	
<Switching characteristics>						
Propagation delay (Low to High)	t_{PLH}	-	20	45	ns	
Propagation delay (High to Low)	t_{PHL}	-	20	45	ns	
Propagation distortion	$\|t_{PLH} - t_{PHL}\|$	-	0	8	ns	
Rise time	t_r	-	2.5	-	ns	
Fall time	t_f	-	2.5	-	ns	
Common-mode transient immunity	CM_L	-	35	-	kV/μs	design assurance

● **Input/Output Timing**

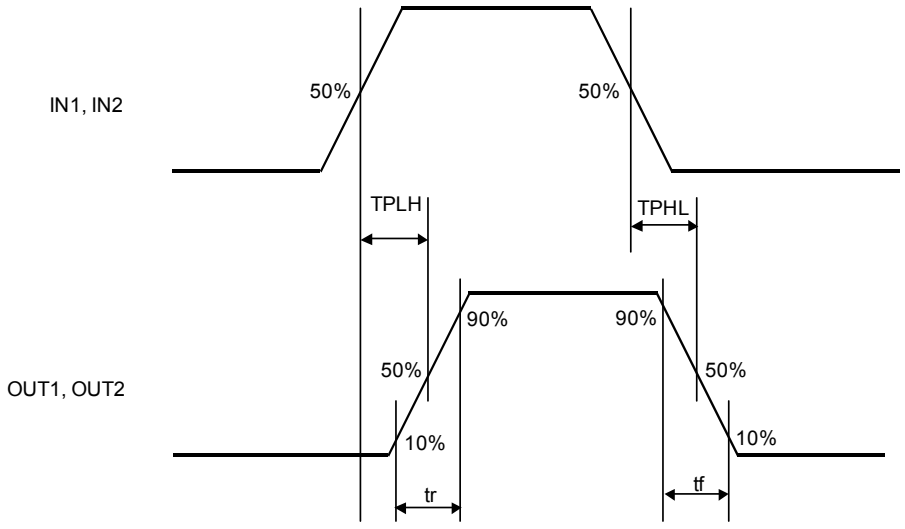


Figure 12. Input/Output Timing Chart

●**Typical Performance Characteristics**

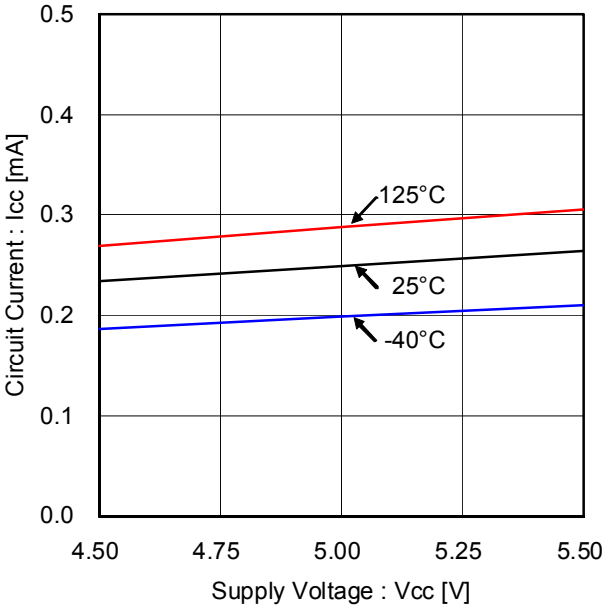


Figure 13. VCC1 Power supply current

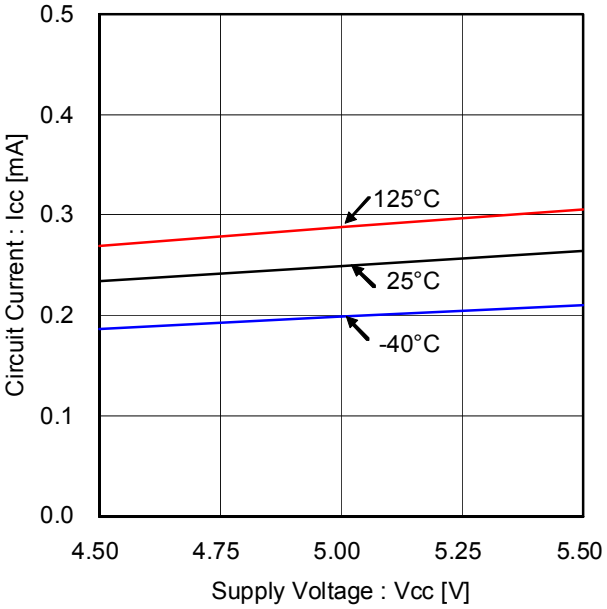


Figure 14. VCC2 Power Supply Current, DC

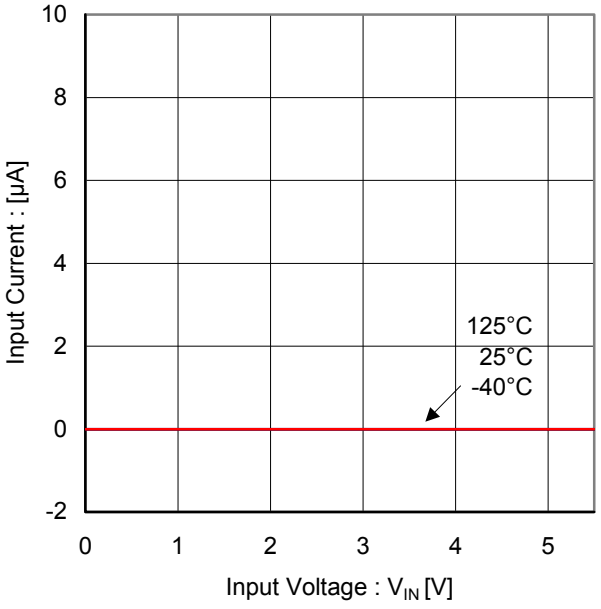


Figure 15. Input Current at Input Pin

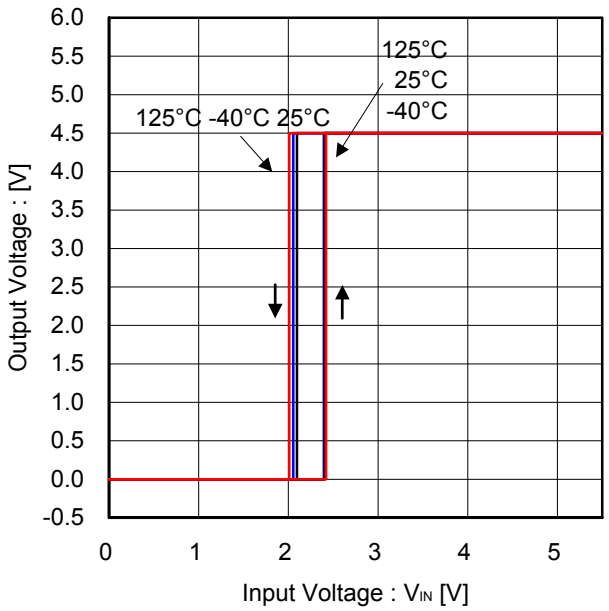


Figure 16. High-/Low-level Input threshold
VCC1,VCC2＝4.5V

●**Typical Performance Characteristics**

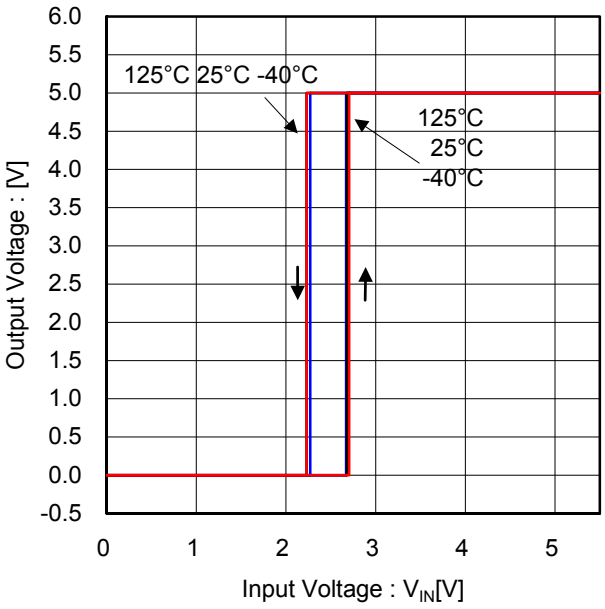


Figure 17. High-/Low-level Input threshold VCC1,VCC2＝5.0V

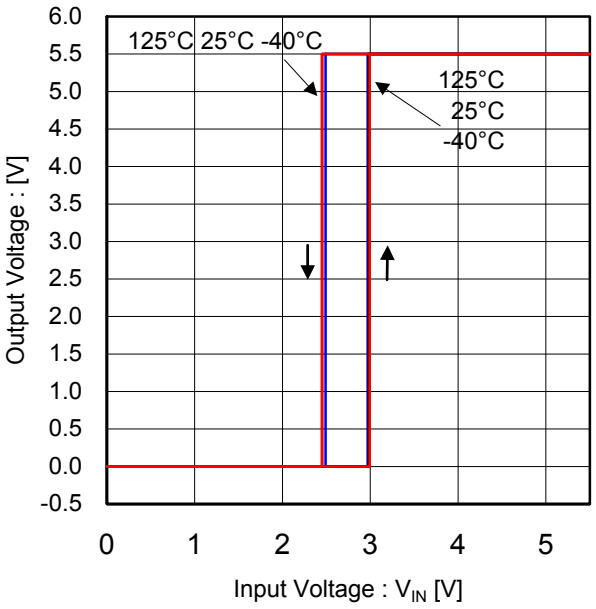


Figure 18. High-/Low-level Input threshold VCC1,VCC2＝5.5V

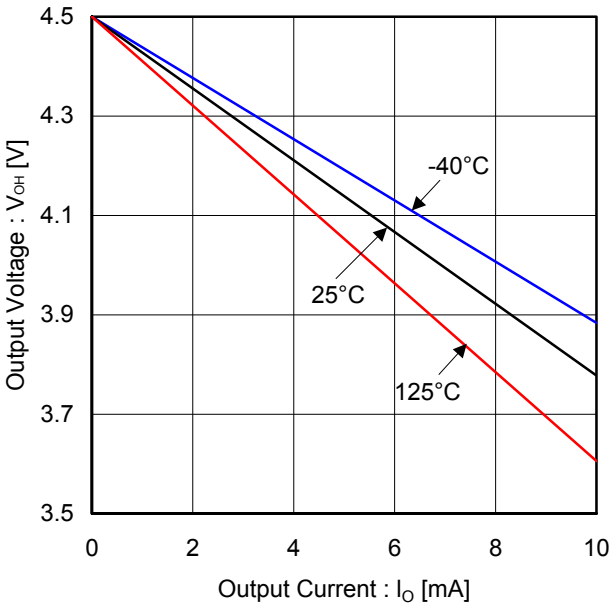


Figure 19. High-level Output Voltage VCC1,VCC2＝4.5V

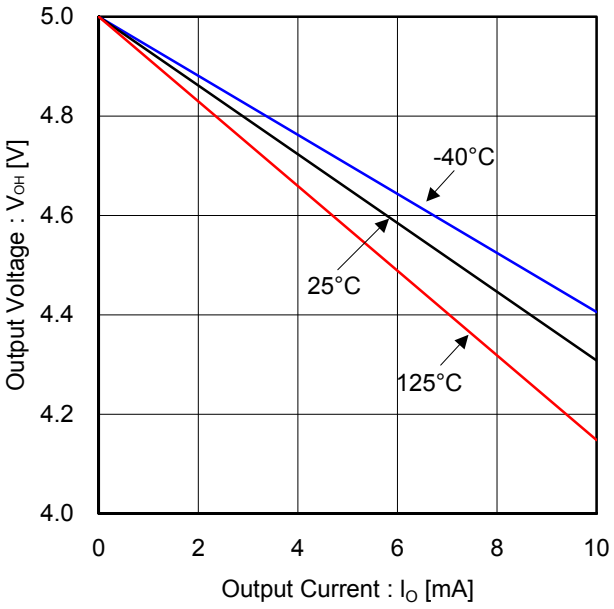


Figure 20. High-level Output Voltage VCC1,VCC2＝5.0V

●**Typical Performance Characteristics**

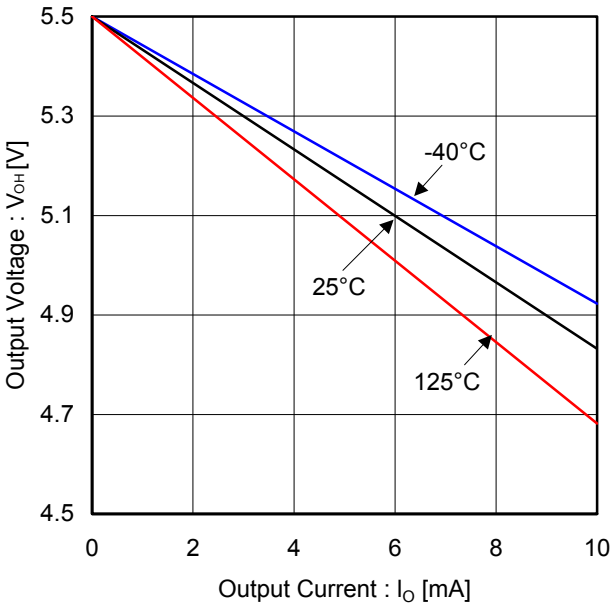


Figure 21. High-level Output Voltage
VCC1,VCC2=5.5V

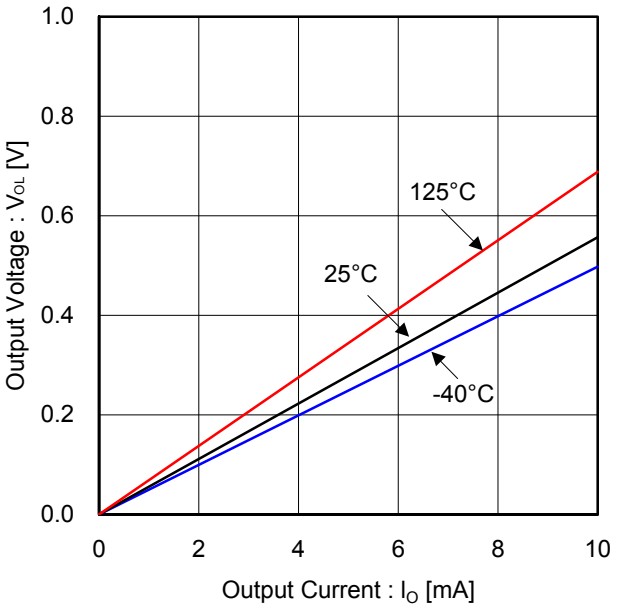


Figure 22. Low-level Output Voltage
VCC1,VCC2=4.5V

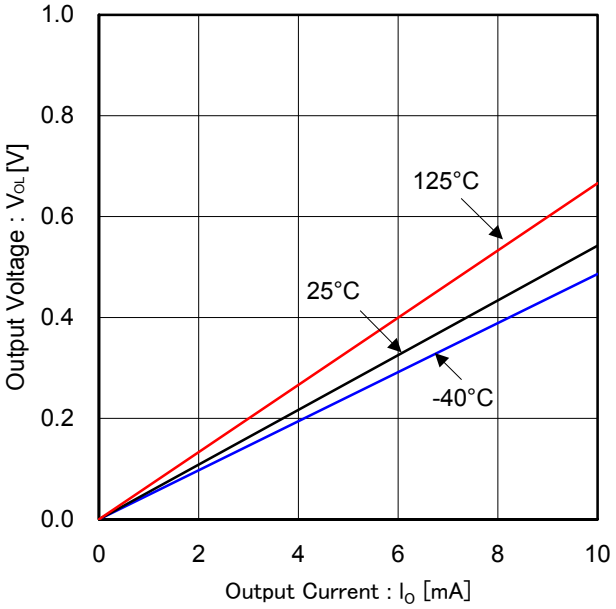


Figure 23. Low-level Output Voltage
VCC1,VCC2=5.0V

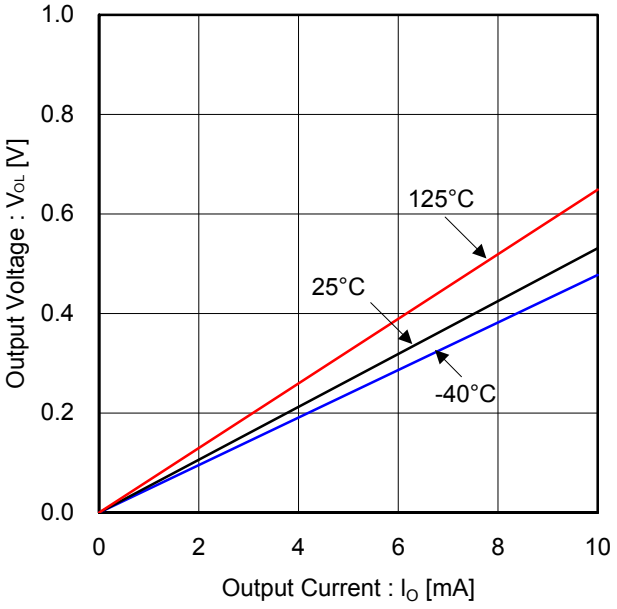


Figure 24. Low-level Output Voltage
VCC1,VCC2=5.5V

●Typical Performance Characteristics

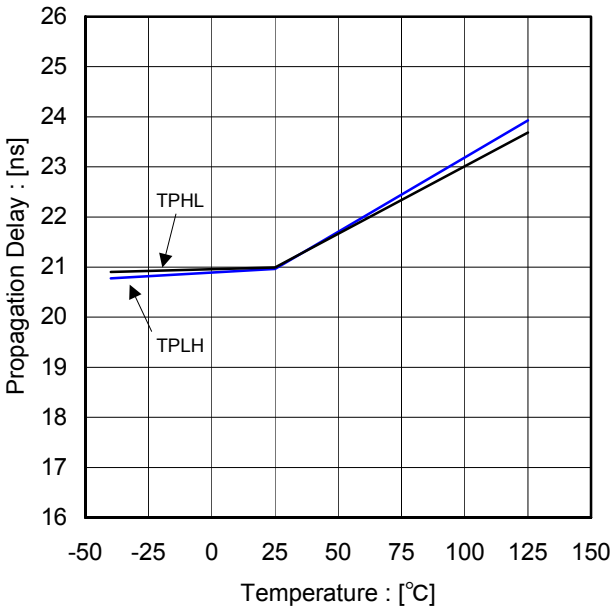


Figure 25. Propagation delay vs. Temperature characteristics VCC1, VCC2 = 4.5V

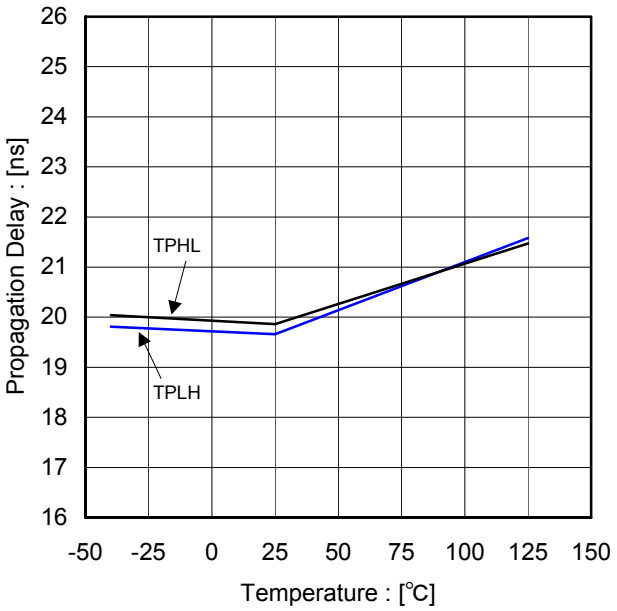


Figure 26. Propagation delay vs. Temperature characteristics VCC1, VCC2 = 5.0V

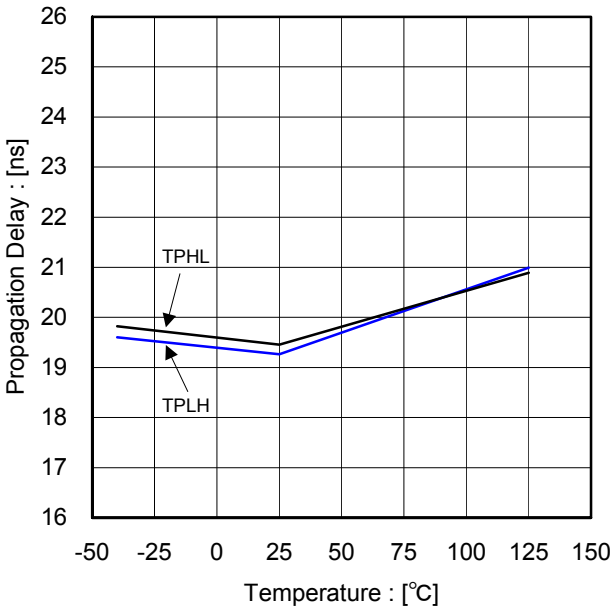


Figure 27. Propagation delay vs. Temperature characteristics VCC1, VCC2 = 5.5V

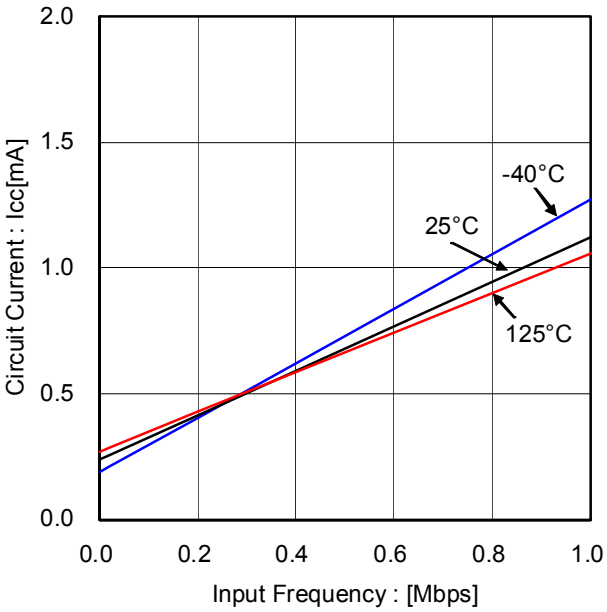


Figure 28. VCC1 Power Supply Current VCC1, VCC2 = 4.5V

●**Typical Performance Characteristics**

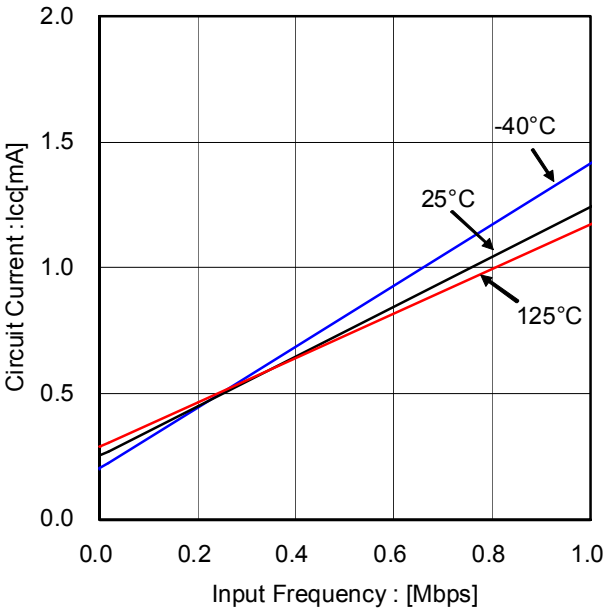


Figure 29. VCC1 Power Supply Current
VCC1, VCC2 = 5.0V

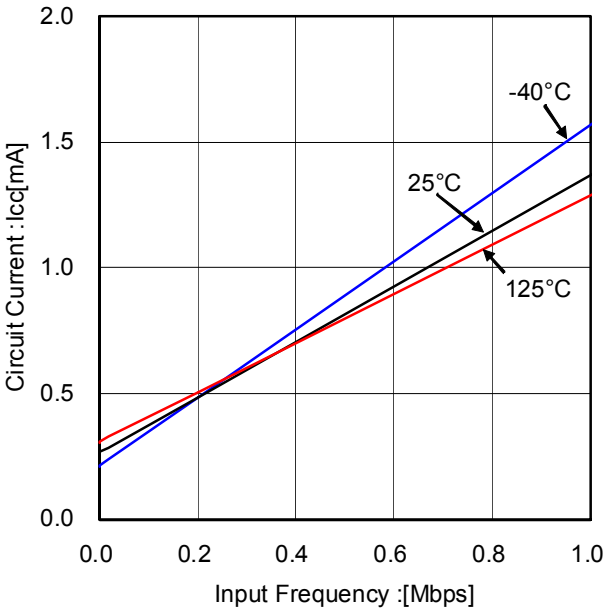


Figure 30. VCC1 Power Supply Current
VCC1, VCC2 = 5.5V

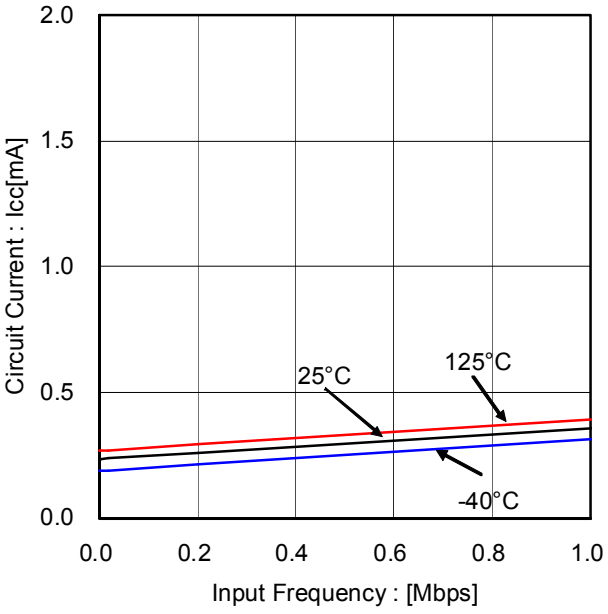


Figure 31. VCC2 Power Supply Current
VCC1, VCC2 = 4.5V

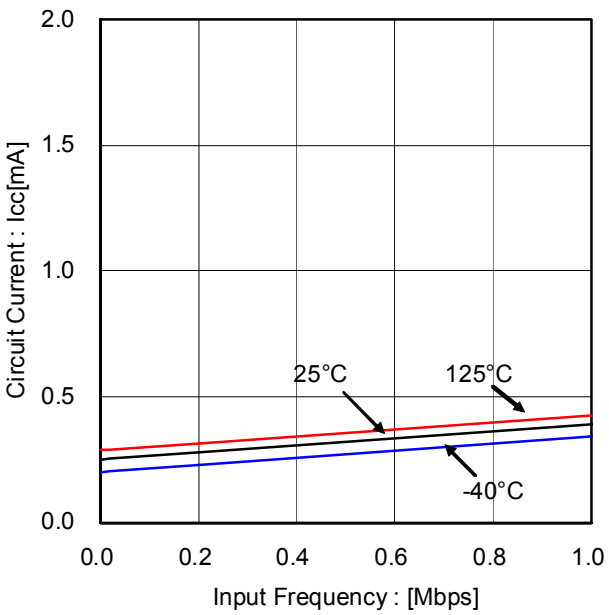


Figure 32. VCC2 Power Supply Current
VCC1, VCC2 = 5.0V

●**Typical Performance Characteristics**

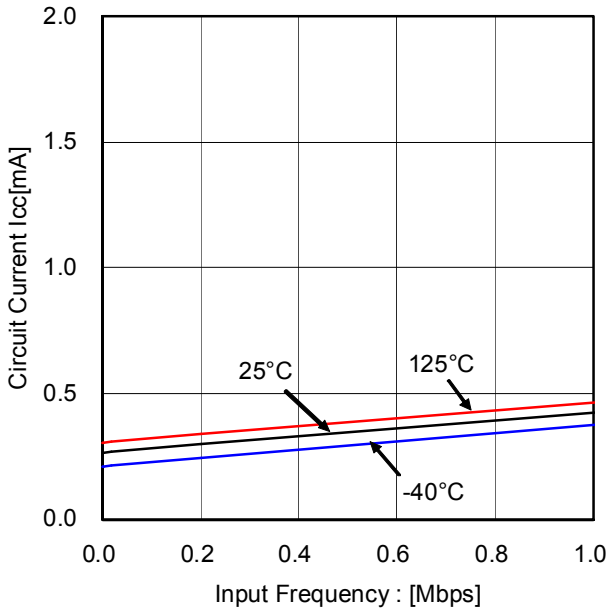


Figure 33. VCC2 Power Supply Current
VCC1, VCC2 =5.5V

●**Interfaces**

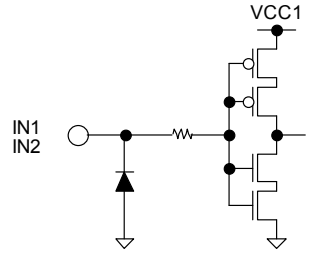


Figure 34. IN1, IN2

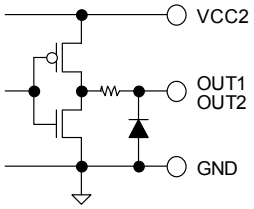


Figure 35. OUT1, OUT2

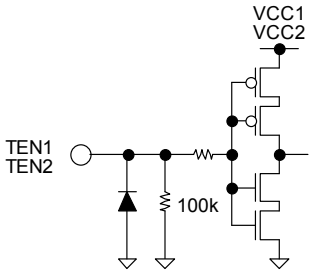


Figure 36. TEN1, TEN2

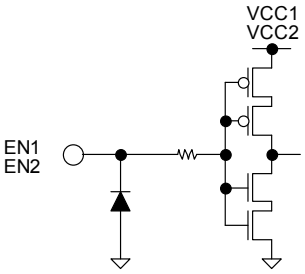


Figure 37. EN1, EN2

●**Power Dissipation Reduction Characteristics**

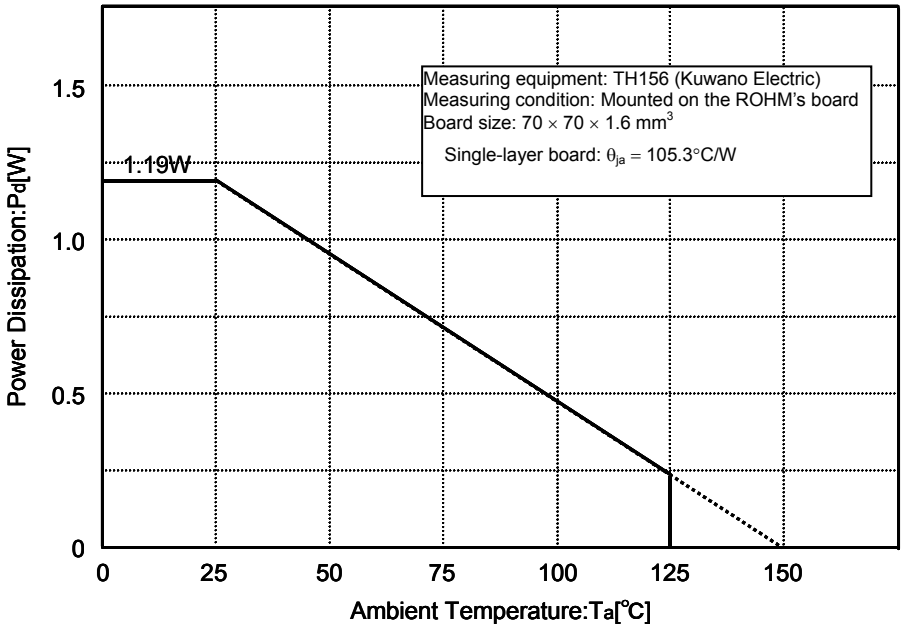


Figure 38. SSOP-B20W Power Dissipation Reduction Curve

●**Thermal Dissipation**

In consideration of the power consumption (P), package power (Pd), and ambient temperature (Tj) of this IC, ensure that the chip temperature of the IC has not exceeded 150°C. If Tj exceeds 150°C, the function as a semiconductor will be disabled to cause problems such as the malfunctions of parasitic elements and increase in leakage current. Constantly using the IC under the said conditions may deteriorate the IC and further lead to its breakdown. Strictly keep Tjmax at 150°C under any circumstances.

●Usage Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND1,GND2 Potential

The potential of GND1 pin must be minimum potential in all operating conditions. (Input side ; 2pin to 9pin)
The potential of GND2 pin must be minimum potential in all operating conditions. (Input side ; 11pin to 20pin)

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(7) Operation in a strong electric field

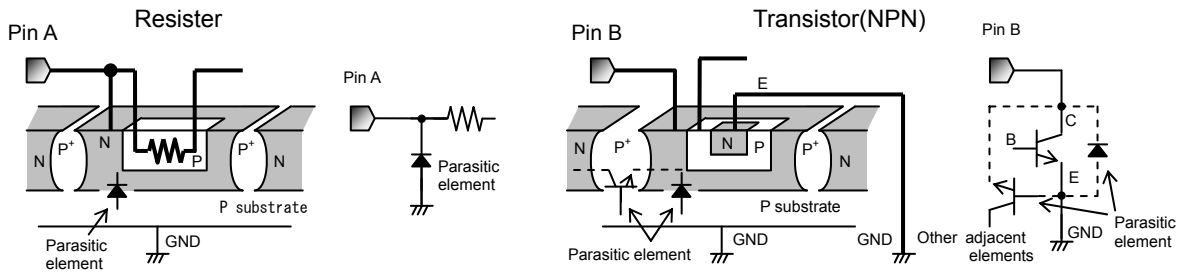
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(9) Input terminal of IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements, in order to keep them isolated.
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, do not use methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



Appendix: Example of monolithic IC structure

(11) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

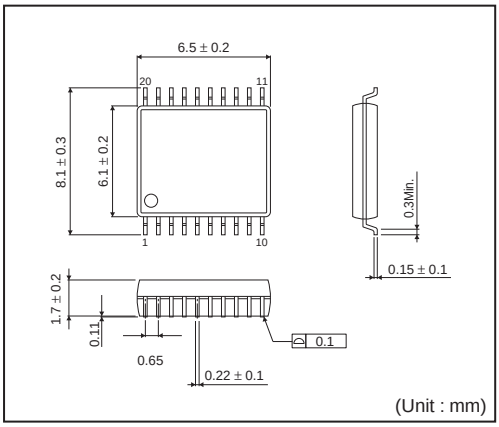
●Ordering Information

B M 6 7 2 2 0 F V	-	CE 2

- Part Number
- Package FV : SSOP-B20W
- Packaging and forming specification E2: Embossed tape and reel

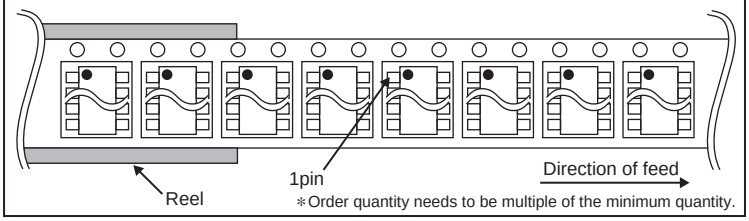
●Physical Dimension Tape and Reel Information

SSOP-B20W



<Tape and Reel information>

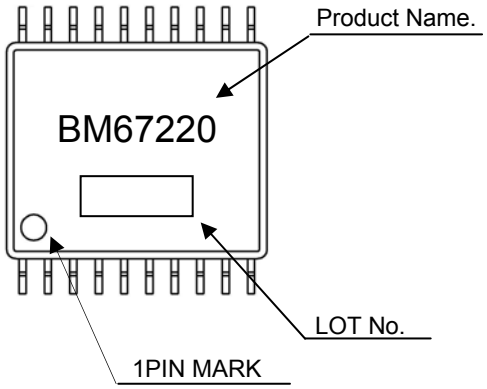
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

SSOP-B20W
TOP VIEW



●改訂履歴

Date	Revision	Changes
25.Jun.2012	001	New Release
26.Oct.2012	002	P.3 Fix typo about 4) Under voltage lock out. P.7 Fix typo about figure 8.sequence. P.10 Fix typo about Electrical Characteristics about IN1,IN2 Input inhibition area.
20.Dec.2012	003	P.5~P.8 Fix typo about input inhibition area. P.21 Delete description.