

Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM6105FW-LBZ

General Description

The BM6105 is a gate driver with isolation voltage 2500Vrms, I/O delay time of 120ns, and minimum input pulse width of 60ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, thermal protection function, and desaturation protection (DESAT) function.

Features

- Providing Galvanic Isolation
- Miller Clamp Function
- Fault signal output function
- Ready signal output function
- Undervoltage lockout function
- Desaturation protection function
- Supporting Negative VEE2

Applications

- Driving IGBT Gate
- Driving MOSFET Gate

Key Specifications

■ Isolation voltage:	2500Vrms
■ Maximum gate drive voltage:	20V
■ I/O delay time:	95ns (Max.)
■ Minimum input pulse width:	60ns (Max.)

Package

SOP16WM

W(Typ) x D(Typ) x H(Max)
10.34mm x 10.31mm x 2.64mm

Typical Application Circuit

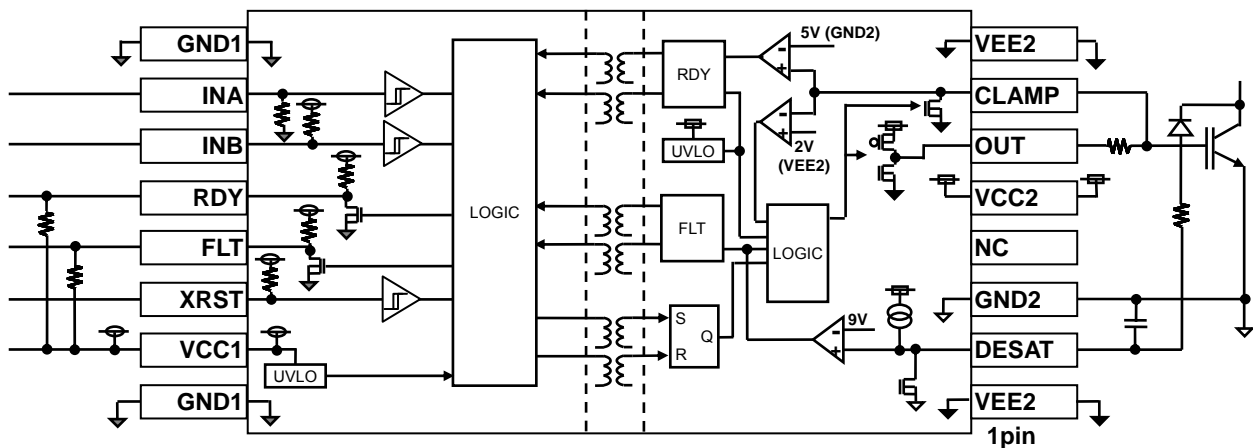


Figure 1. Typical application circuit

Recommended range of external constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
VCC1	C _{VCC1}	0.1	1.0	-	μF
VCC2	C _{VCC2}	0.33	-	-	μF

Pin Configurations

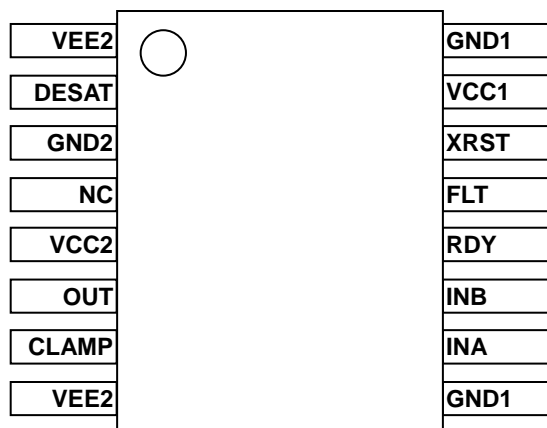


Figure 2. Pin configuration

Pin Descriptions

Pin No.	Pin Name	Function
1	VEE2	Output-side negative power supply pin
2	DESAT	Desaturation protection pin
3	GND2	Output-side ground pin
4	NC	No connect
5	VCC2	Output-side positive power supply pin
6	OUT	Output pin
7	CLAMP	Miller clamp pin
8	VEE2	Output-side negative power supply pin
9	GND1	Input-side ground pin
10	INA	Control input pin
11	INB	Opposite driver's control input pin
12	RDY	Ready output pin
13	FLT	Fault output pin
14	XRST	Reset input pin
15	VCC1	Input-side power supply pin
16	GND1	Input-side ground pin

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3 to +7.0 ^(Note1)	V
Output-side positive supply voltage	V_{CC2}	-0.3 to +24.0 ^(Note2)	V
Output-side negative supply voltage	V_{EE2}	-15.0 to +0.3 ^(Note3)	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	30.0	V
INA, INB, XRST pin input voltage	V_{IN}	-0.3 to +VCC1+0.3 or 7.0 ^(Note1)	V
RDY, FLT pin input voltage	V_{FLT}	-0.3 to +VCC1+0.3 or 7.0 ^(Note1)	V
DESAT pin input voltage	$V_{DESATIN}$	-0.3 to VCC2+0.3 ^(Note2)	V
OUT pin output current (10 μ s)	$I_{OUTPEAK}$	5.0	A
OUT, CLAMP pin voltage		VEE2-0.3V to VCC2+0.3V	V
RDY, FLT output current	I_{FLT}	10	mA
Power dissipation	P_d	TBD ^(Note4)	W
Operating temperature range	T_{opr}	-40 to +105	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Junction temperature	T_{jmax}	+150	°C

(Note1) Relative to GND1.

(Note2) Relative to GND2.

(Note3) Should not exceed Pd and Tj=150°C.

(Note4) Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Input-side supply voltage	V_{CC1} ^(Note5)	4.5	5.5	V
Output-side positive supply voltage	V_{CC2} ^(Note6)	12.6	20.0	V
Output-side negative supply voltage	V_{EE2} ^(Note6)	-12	0	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	-	28.0	V

(Note5) Relative to GND1.

(Note6) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V _{IO} =500V)	R_s	>10 ⁹	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{EE2}	3000	Vrms

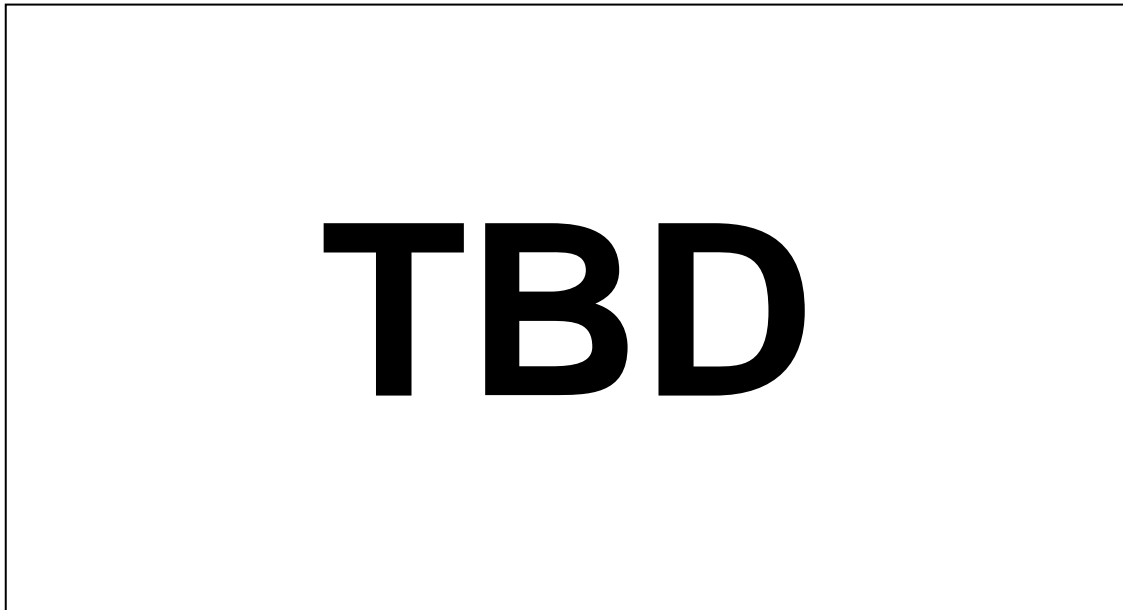
Electrical Characteristics(Unless otherwise specified $T_a = -40^{\circ}\text{C}$ to 105°C , $V_{CC1} = 4.5\text{V}$ to 5.5V , $V_{CC2} = 12.6\text{V}$ to 20V , $V_{EE2} = -12\text{V}$ to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.16	0.32	0.48	mA	
Input side circuit current 2	I_{CC12}	0.21	0.42	0.63	mA	INA=10kHz, Duty=50%
Input side circuit current 3	I_{CC13}	0.26	0.52	0.78	mA	INA=20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	0.9	1.8	2.7	mA	OUT=L
Output side circuit current 2	I_{CC22}	0.8	1.7	2.5	mA	OUT=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB, XRST
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB, XRST
Logic pull-down resistance	R_{IND}	25	50	100	k Ω	INA
Logic pull-up resistance	R_{INU}	25	50	100	k Ω	INB, XRST, RDY, FLT
Logic input mask time	t_{INMSK}	-	-	60	ns	INA, INB
Minimum XRST pulse width	$t_{XRSTMIN}$	800	-	-	ns	
Output						
OUT ON resistance (Source)	R_{ONH}	0.3	0.8	1.5	Ω	$I_{OUT} = 40\text{mA}$
OUT ON resistance (Sink)	R_{ONL}	0.2	0.4	0.7	Ω	$I_{OUT} = 40\text{mA}$
OUT maximum current	I_{OUTMAX}	3.0	4.5	-	A	Guaranteed by design
CLAMP ON resistance	R_{ONPRO}	0.2	0.4	0.7	Ω	$I_{CLAMP} = 40\text{mA}$
Low level CLAMP current	I_{CLAMPL}	3.0	4.5	-	A	Guaranteed by design
Turn ON time	t_{PON}	45	70	95	ns	
Turn OFF time	t_{POFF}	45	70	95	ns	
Propagation distortion	t_{PDIST}	-20	0	20	ns	$t_{POFF} - t_{PON}$
Rise time	t_{RISE}	-	50	100	ns	10 Ω , 10nF between OUT-VEE2
Fall time	t_{FALL}	-	50	100	ns	Guaranteed by design
CLAMP ON threshold voltage	V_{CLPON}	1.8	2	2.2	V	Relative to VEE2

Electrical Characteristics - continued(Unless otherwise specified $T_a = -40^\circ\text{C}$ to 105°C , $V_{CC1} = 4.5\text{V}$ to 5.5V , $V_{CC2} = 12.6\text{V}$ to 20V , $V_{EE2} = -12\text{V}$ to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	1.0	2.5	5.0	μs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	11.4	12.0	12.6	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	10.4	11.0	11.6	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	1.0	2.0	3.0	μs	
DESAT source current	I_{DESAT}	450	500	550	μA	
DESAT threshold voltage	V_{DESAT}	8.5	9.0	9.5	mV	
DESAT filter time	$t_{DESATFIL}$	0.15	0.22	0.27	μs	
DESAT delay time (OUT)	$t_{DESATOUT}$	0.22	0.30	0.38	μs	
DESAT delay time (FLT)	$t_{DESATFLT}$	0.22	0.30	0.38	μs	
DESAT low voltage	V_{DESATL}	-	0.1	0.22	V	$I_{DESAT} = 1\text{mA}$
Leading edge blanking	$t_{DESATLEB}$	0.28	0.4	0.52	μs	Guaranteed by design
OSFB threshold voltage H	V_{OSFBH}	4.5	5.0	5.5	V	Relative to GND2
OSFB threshold voltage L	V_{OSFBL}	4.0	4.5	5.0	V	Relative to GND2
OSFB filter time	$t_{OSFBFIL}$	1.5	2.0	2.6	μs	
RDY output low voltage	V_{RDYL}	-	0.15	0.30	V	$I_{RDY} = 5\text{mA}$
FLT output low voltage	V_{FLTL}	-	0.15	0.30	V	$I_{FLT} = 5\text{mA}$

Typical Performance Curves



Description of pins and cautions on layout of board

1. VCC1 (Input-side power supply pin)

The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2. GND1 (Input-side ground pin)

The GND1 pin is a ground pin on the input side.

3. VCC2 (Output-side positive power supply pin)

The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4. VEE2 (Output-side negative power supply pin)

The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. To use no negative power supply, connect the VEE2 pin to the GND2 pin.

5. GND2 (Output-side ground pin)

The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

6. INA, INB and XRST (Control input terminal)

The INA, INB and XRST pin is a pin used to determine output logic. And XRST is in charge of setting back the FLT pin.

XRST	INB	INA	OUT
L	X	X	L
H	H	X	L
H	L	L	L
H	L	H	H

7. FLT (Fault output pin)

The FLT pin is an open drain pin used to output a fault signal when desaturation function is activated, and will be cleared at the rising edge of FLT.

Status	FLT
While in normal operation	H
When desaturation function is activated	L

8. RDY (Ready output pin)

The RDY pin shows the status of three internal protection features which are VCC1 UVLO, VCC2 UVLO, and output state feedback (OSFB). The term 'output state feedback' shows whether CLAMP pin voltage (High or Low) corresponds to input logic or not.

Status	RDY
While in normal operation	H
VCC1 UVLO or VCC2 UVLO or Output state feedback	L

9. OUT (Output pin)

The OUT pin is a pin used to drive the gate of a power device.

10. CLAMP (Miller clamp pin)

The CLAMP pin is a pin for preventing increase in gate voltage due to the miller current of the power device connected to OUT pin. And this pin is monitoring the gate voltage of IGBT/MOSFET.

11. DESAT (Desaturation protection pin)

The DESAT pin is a pin used to detect desaturation of IGBT/MOSFET. When the DESAT pin voltage exceeds V_{DESAT} , the DESAT function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the DESAT pin to the GND2 pin if the desaturation protection is not used. In order to prevent the wrong detection due to noise, the noise mask time $t_{DESATFIL}$ is set.

Description of functions and examples of constant setting

1. Gate voltage rise prevention function

If OUT=L and the CLAMP pin voltage < V_{CLPON}, the internal MOSFET of the CLAMP pin turns on, and if not, the CLAMP pin turns off.

OUT	CLAMP	Internal MOSFET of the CLAMP pin
L	Less than V _{CLPON}	ON
L	Not less than V _{CLPON}	OFF
H	X	OFF

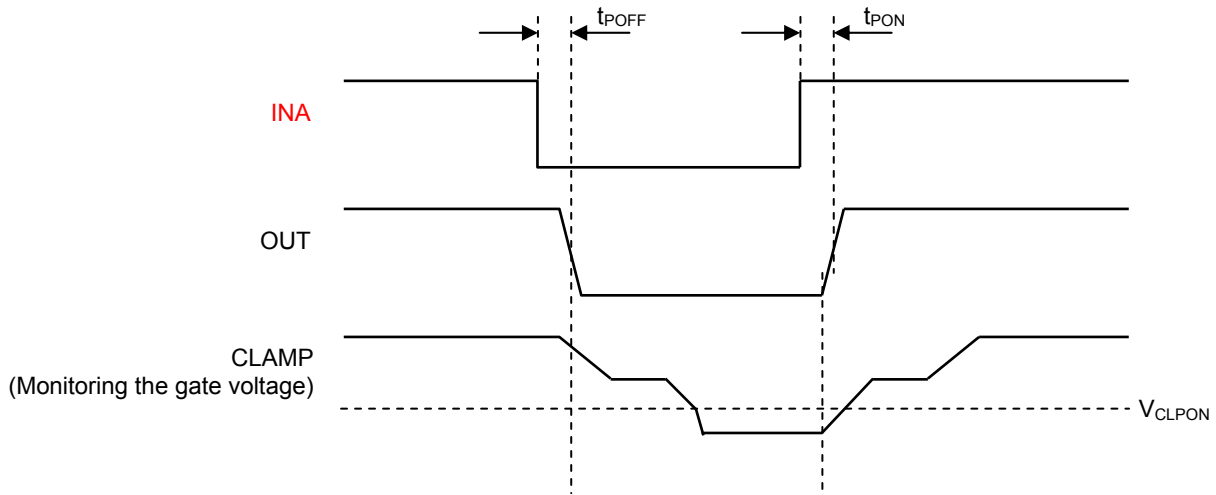


Figure 3. Timing chart of Miller clamp function

2. Fault status output

This function is used to output a fault signal from the FLT pin when the desaturation protection function is activated and hold the Fault signal until rising edge of XRST is put in.

3. Undervoltage Lockout (UVLO) function

The **BM6105FW-LBZ** incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage, the OUT pin and the RDY pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. To prevent malfunctions due to noises, mask time t_{UVLO1MSK} and t_{UVLO2MSK} are set on both low and high voltage sides.

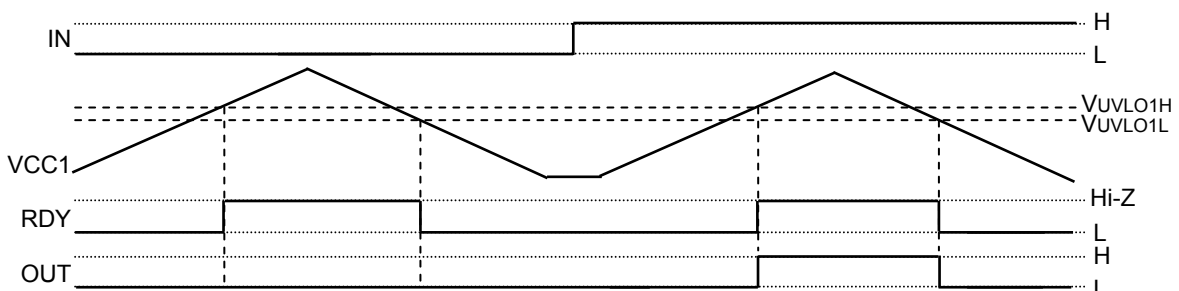


Figure 4. Input-side UVLO Function Operation Timing Chart

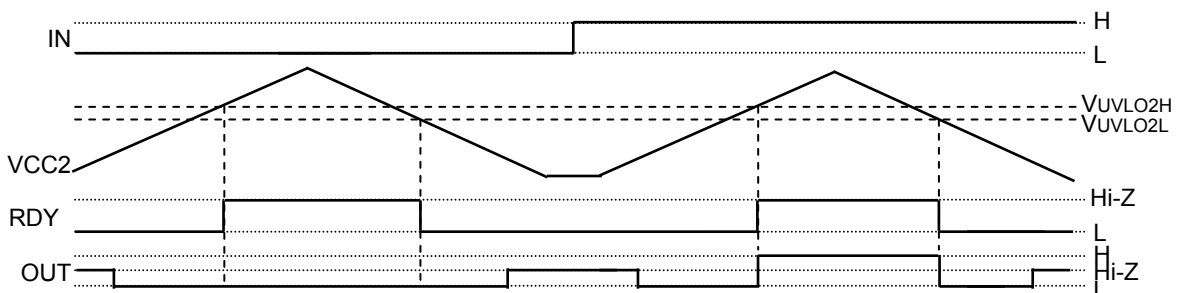


Figure 5. Output-side UVLO Operation Timing Chart

4. Desaturation protection function (DESAT)

When the DESAT pin voltage exceeds V_{DESAT} , the DESAT function will be activated. When the DESAT function is activated, the OUT pin voltage will be set to the “L” level, and then the FLT pin voltage to the “L” level. When the rising edge is put in the XRST pin, the DESAT function will be released.

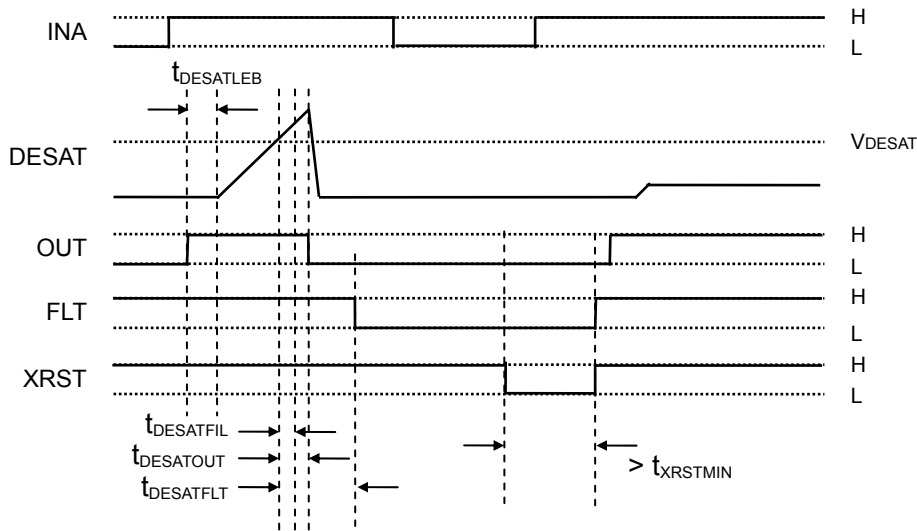


Figure 6. DESAT Operation Timing Chart

5.I/O condition table

No.	Status	Input							Output			
		VCC1	VCC2	DESAT	XRST	INB	INA	CLAMP	OUT	CLAMP	FLT	RDY
1	VCC1UVLO	UVLO	X	X	X	X	X	H	L	Hi-Z	H	L
2		UVLO	X	X	X	X	X	L	L	L	H	L
3	VCC2UVLO	O	UVLO	L	X	X	X	H	L	Hi-Z	H	L
4		O	UVLO	L	X	X	X	L	L	L	H	L
5		O	UVLO	H	X	X	X	H	L	Hi-Z	L	L
6		O	UVLO	H	X	X	X	L	L	L	L	L
7	DESAT	O	O	H	X	X	X	H	L	Hi-Z	L	H(*)
8		O	O	H	X	X	X	L	L	L	L	H(*)
9	XRST	O	O	L	L	X	X	H	L	Hi-Z	H	H(*)
10		O	O	L	L	X	X	L	L	L	H	H(*)
11		O	O	L	H	H	X	H	L	Hi-Z	H	H(*)
12	Normal operation	O	O	L	H	H	X	L	L	L	H	H(*)
13		O	O	L	H	L	L	H	L	Hi-Z	H	H(*)
14		O	O	L	H	L	L	L	L	L	H	H(*)
15		O	O	L	H	L	H	X	H	Hi-Z	H	H(*)

O: VCC1 or VCC2 > UVLO, X:Don't care

(*) If the IGBT/MOSFET gate voltage doesn't become the expected value during $t_{OSFBFIL}$, the RDY pin will become “L”. And this stage is cleared automatically if the IGBT/MOSFET gate voltage becomes the expected value.

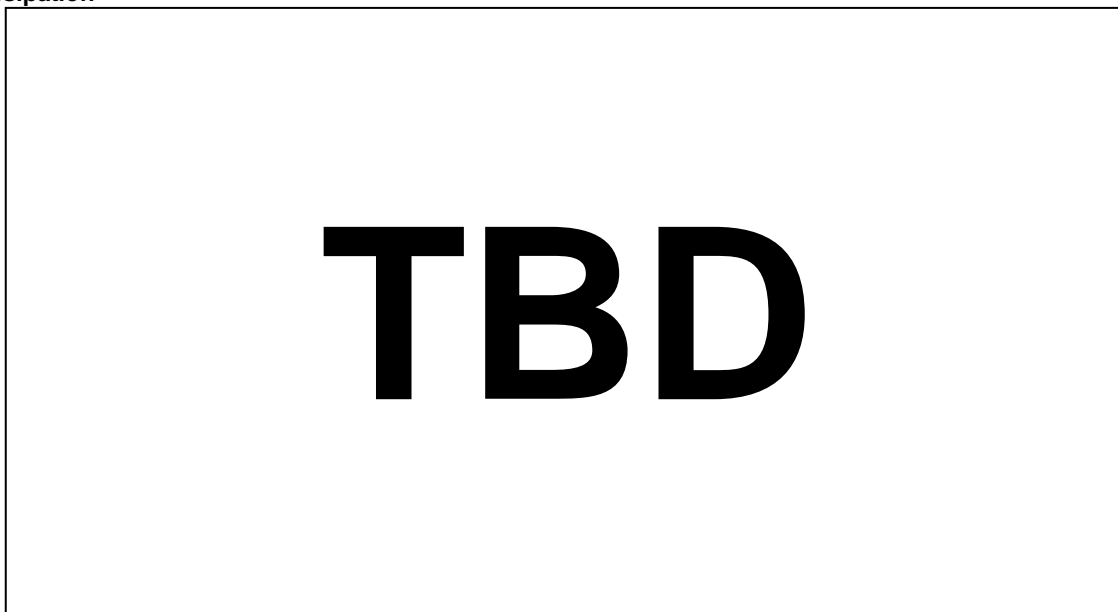
Power Dissipation

Figure 7. SOIC16 Derating Curve

Thermal design

Please confirm that the IC's chip temperature T_j is not over 150°C , while considering the IC's power consumption (W), package power (P_d) and ambient temperature (T_a). When $T_j=150^{\circ}\text{C}$ is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. $T_{j\text{max}}=150^{\circ}\text{C}$ must be strictly obeyed under all circumstances.

I/O equivalence circuits

Pin No.	Name	I/O equivalence circuits
	Function	
2	DESAT	
	Desaturation protection pin	
6	OUT	
	Output pin	
7	CLAMP	
	Miller clamp pin	

Pin No.	Name	I/O equivalence circuits
	Function	
10	INA	
	Control input pin	
11	INB	
	Opposite driver's control input pin	
14	XRST	
	Reset input pin	
12	RDY	
	Ready output pin	
13	FLT	
	Fault output pin	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins of input side (9pin to 16pin) are at a voltage below that of the GND1 pin at any time, even during transient condition.

Ensure that no pins of output side (1pin to 8pin) are at a voltage below that of the VEE2 pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

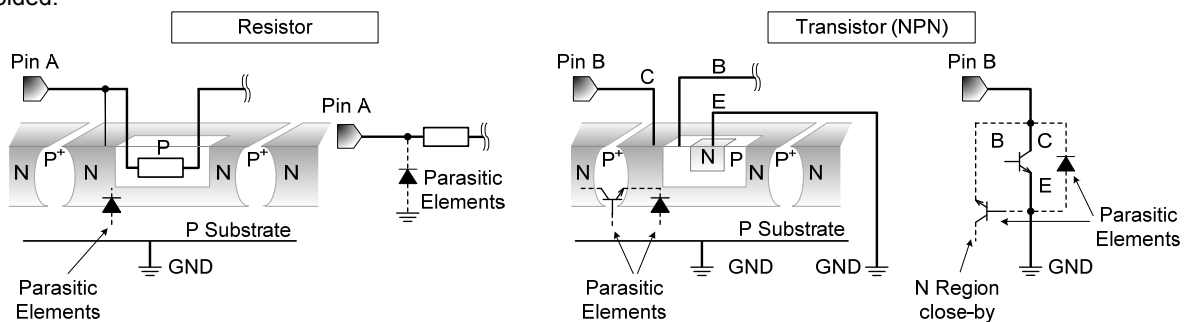


Figure 8. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B M 6 1 0 5 F W - L B Z E 2

Part Number

Package
FW:SOP16WM

Product class
LB for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

Physical Dimension Tape and Reel Information

TBD

Marking Diagram(TOP VIEW)

TBD

Revision History

Date	Revision	Changes
08.Apr.2013	001	New Release
07.Nov.2013	002	Changing Electrical Characteristics Corresponding mistakes

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment, aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.
2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - [a] Installation of protection circuits or other protective devices to improve system safety
 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

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Other Precaution

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