Isolation voltage 2500Vrms
1ch Gate Driver Providing Galvanic Isolation

BM6104FV-C

●General Description

The BM6104FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 150ns, and minimum input pulse width of 90ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, and short current protection (SCP, DESAT) function.

●Features

- Providing Galvanic Isolation
- Active Miller Clamping
- Fault signal output function (Adjustable output holding time)
- Undervoltage lockout function
- Short current protection function (Adjustable reset time)
- Soft turn-off function for short current protection (Adjustable turn-off time)
- Supporting Negative VEE2
- Output state feedback function

●Key Specifications

- Isolation voltage: 2500Vrms
- Maximum gate drive voltage: 24V
- I/O delay time: 150ns(Max.)
- Minimum input pulse width: 90ns(Max.)

●Package

	W(Typ.) x D(Typ.) x H(Max.)
SSOP-B20W	6.50mm x 8.10mm x 2.01mm

●Applications

- Driving IGBT Gate
- Driving MOSFET Gate

●Typical Application Circuits

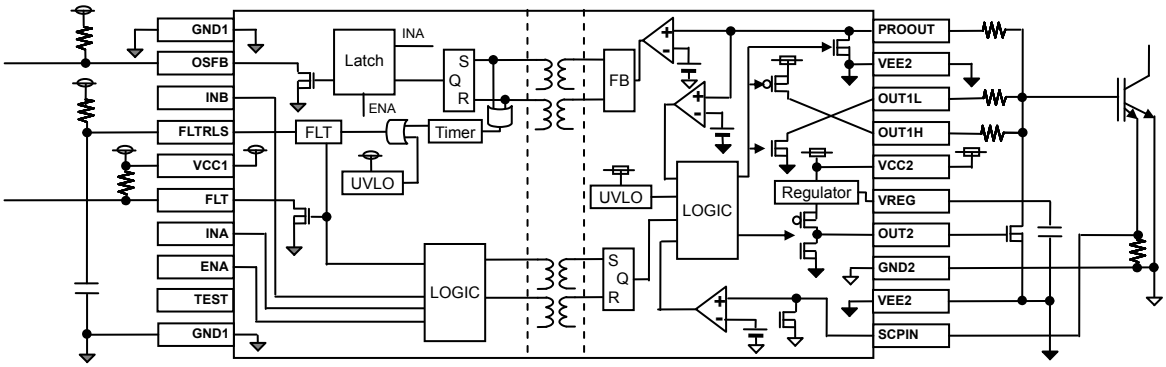


Fig.1 For using 4-pin IGBT (for using SCP function)

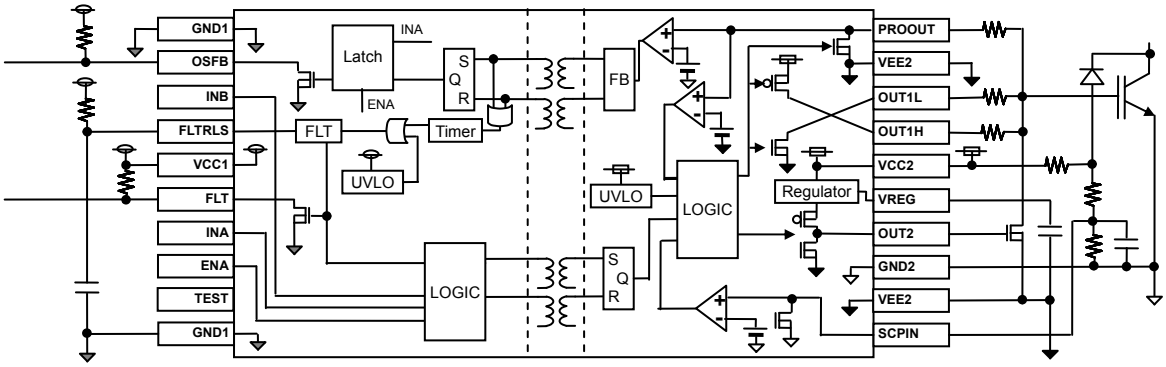


Fig.2 For using 3-pin IGBT (for using DESAT function)

●**Recommended range of external constants**

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
FLTRLS	C_{FLTRLS}	-	0.01	0.47	uF
	R_{FLTRLS}	50	200	1000	kΩ
VREG	C_{VREG}	1.0	3.3	10.0	uF
VCC1	C_{VCC1}	0.1	1.0	-	uF
VCC2	C_{VCC2}	0.33	-	-	uF

●**Pin Configurations**

SSOP-B20W
(TOP VIEW)

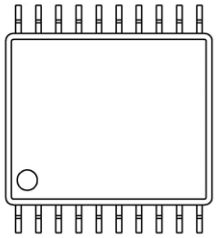


Fig.3 Pin configuration

●**Pin Descriptions**

Pin No.	Pin Name	Function
1	SCPIN	Short current detection pin
2	VEE2	Output-side negative power supply pin
3	GND2	Output-side ground pin
4	OUT2	MOS FET control pin for Miller Clamp
5	VREG	Power supply pin for driving MOS FET for Miller Clamp
6	VCC2	Output-side positive power supply pin
7	OUT1H	Source side output pin
8	OUT1L	Sink side output pin
9	VEE2	Output-side negative power supply pin
10	PROOUT	Soft turn-off pin
11	GND1	Input-side ground pin
12	OSFB	Output state feedback output pin
13	INB	Opposite driver’s control input pin
14	FLTRLS	Fault output holding time setting pin
15	VCC1	Input-side power supply pin
16	FLT	Fault output pin
17	INA	Control input pin
18	ENA	Input enabling signal input pin
19	TEST	Test mode setting pin
20	GND1	Input-side ground pin

●Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side positive power supply pin)
The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT1 pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) VEE2 (Output-side negative power supply pin)
The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT1 pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. To use no negative power supply, connect the VEE2 pin to the GND2 pin.

5) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

6) IN (Control input terminal)
The IN pin is a pin used to determine output logic.

ENA	INB	INA	OUT1
H	X	X	L
L	H	X	L
L	L	L	L
L	L	H	H

7) FLT (Fault output pin)
The FLT pin is an open drain pin used to output a fault signal when a fault occurs (i.e., when the undervoltage lockout function (UVLO) or short current protection function (SCP) is activated).

Pin	FLT
While in normal operation	Hi-Z
When an Fault occurs (When UVLO or SCP is activated)	L

8) FLTRLS (Fault output holding time setting pin)
The FLTRLS pin is a pin used to make setting of time to hold an Fault signal. Connect a capacitor between the FLTRLS pin and the GND1 pin, and a resistor between it and the VCC1 pin.
The Fault signal is held until the FLTRLS pin voltage exceeds a voltage set with the V_{FLTRLS} parameter. To set holding time to 0 ms, do not connect the capacitor. Short-circuiting the FLTRLS pin to the VCC1 pin will cause a high current to flow in the FLTRLS pin and, in an open state, may cause the IC to malfunction. To avoid such trouble, be sure to connect a resistor between the FLTRLS and the VCC1 pins.

9) OUT1H, OUT1L (Output pin)
The OUT1H pin is a source side pin used to drive the gate of a power device, and the OUT1L pin is a sink side pin used to drive the gate of a power device.

10) OUT2 (MOS FET control pin for Miller Clamp)
The OUT2 pin is a pin for controlling the external MOS switch for preventing increase in gate voltage due to the miller current of the power device connected to OUT1 pin.

11) VREG (Power supply pin for driving MOS FET for Miller Clamp)
The VREG pin is a power supply pin for Miller Clamp. Be sure to connect a capacitor between VREG pin and VEE2 pin for preventing the oscillation and to reduce voltage fluctuations due to OUT2 pin output current.

12) PROOUT (Soft turn-off pin)
The PROOUT pin is a pin used to put the soft turn-off function of a power devise in operation when the SCP function is activated. This pin combines with the gate voltage monitoring pin for Miller Clamp function and OSFB function which output the gate state.

13) SCPIN (Short current detection pin)
The SCPIN pin is a pin used to detect current for short current protection. When the SCPIN pin voltage exceeds V_{SCDET}, the SCP function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the SCPIN pin to the GND2 pin if the short current protection is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{SCPMSK} is set.

14) OSFB (Output state feedback output pin)

The OSFB pin is an open drain pin used to output the gate state. If the INA pin and the OUT1 pin are at the same level, the OSFB pin output the “Hi-Z” level, otherwise the OSFB pin output the “L” level and hold “L” until ENA=H or UVLO on low voltage side is activated.

●Description of functions and examples of constant setting

1) Miller Clamp function

When OUT1=L and PROOUT pin voltage < V_{OUT2ON}, H is output from OUT2 pin and the external MOS switch is turned ON. When OUT1=H, L is output from OUT2 pin and the external MOS switch is turned OFF. While the short-circuit protection function is activated, L is output from OUT2 pin and the external MOS switch is turned OFF.

Short current	SCPIN	IN	PROOUT	OUT2
Detected	Not less than V_{SCDET}	X	X	L
Not detected	X	L	Not less than V_{OUT2ON}	L
	X	L	less than V_{OUT2ON}	H
	X	H	X	L

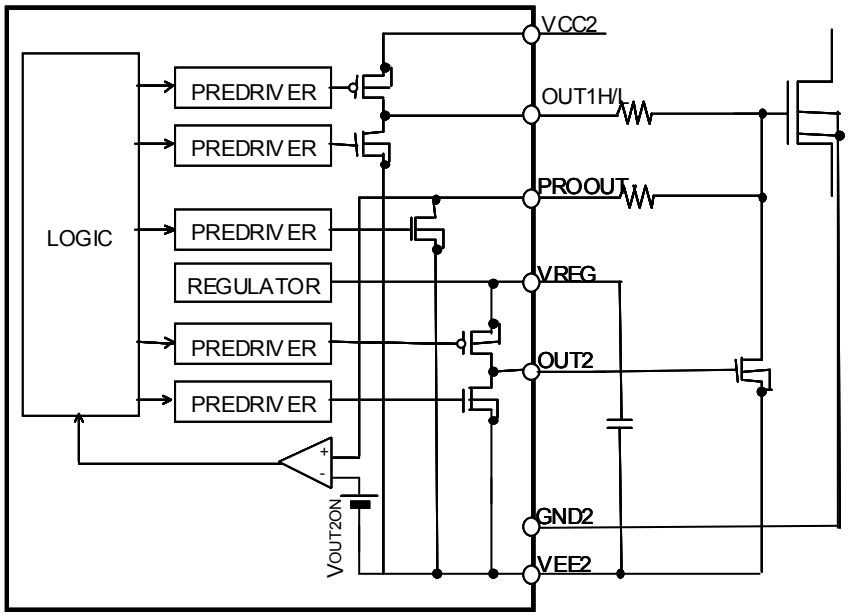


Fig.4 Block diagram of Miller Clamp function.

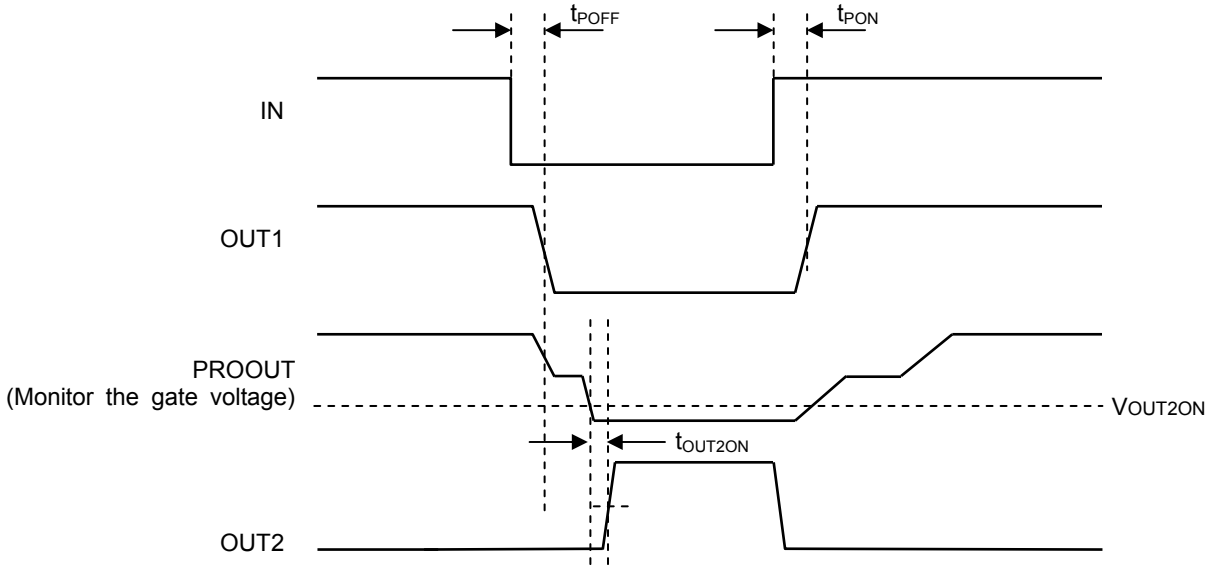


Fig.5 Timing chart of Miller Clamp function

2) Fault status output

This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the undervoltage lockout function (UVLO) or short current protection function (SCP) is activated) and hold the Fault signal until the set Fault output holding time is completed. The Fault output holding time t_{FLTRLS} is given as the following equation with the settings of capacitor C_{FLTRLS} and resistor R_{FLTRLS} connected to the FLTRLS pin. For example, when C_{FLTRLS} is set to 0.01μF and R_{FLTRLS} is set to 200kΩ, the holding time will be set to 2 ms.

t_{FLTRLS} [ms]= C_{FLTRLS} [μF]•R_{FLTRLS} [kΩ]

To set the fault output holding time to “0” ms, only connect the resistor R_{FLTRLS}.

Status	FLT pin
Normal	Hi-Z
Fault occurs	L

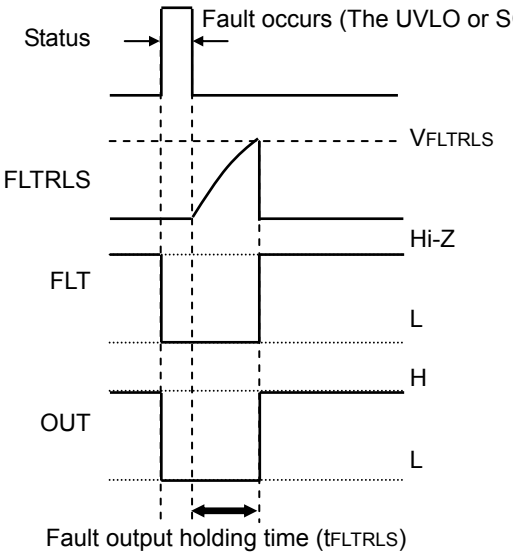


Fig. 6 Fault Status Output Timing Chart

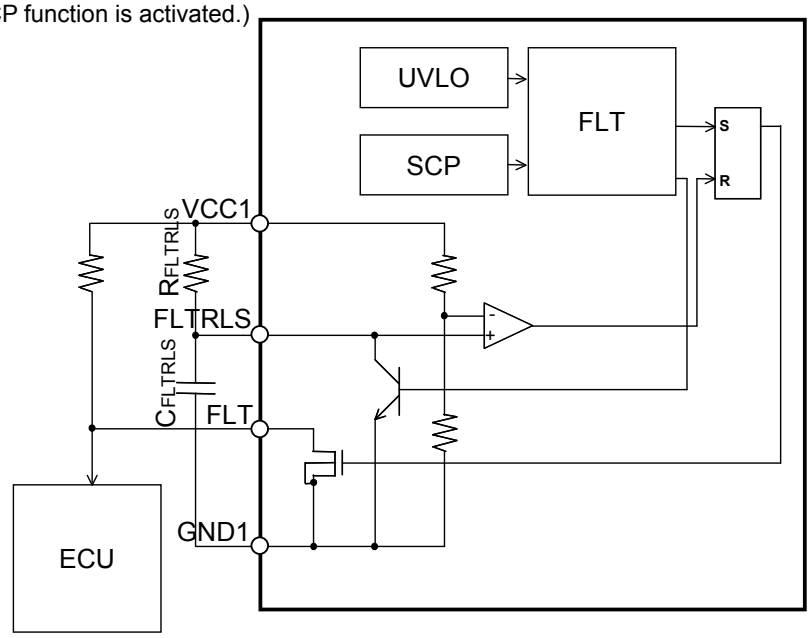


Fig. 7 Fault Output Block Diagram

3) Undervoltage Lockout (UVLO) function

The BM6104FV-C incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage, the OUT pin and the FLT pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. However, during the fault output holding time set in “2) Fault status output” section, the OUT pin and the FLT pin will hold the “L” signal. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both low and high voltage sides.

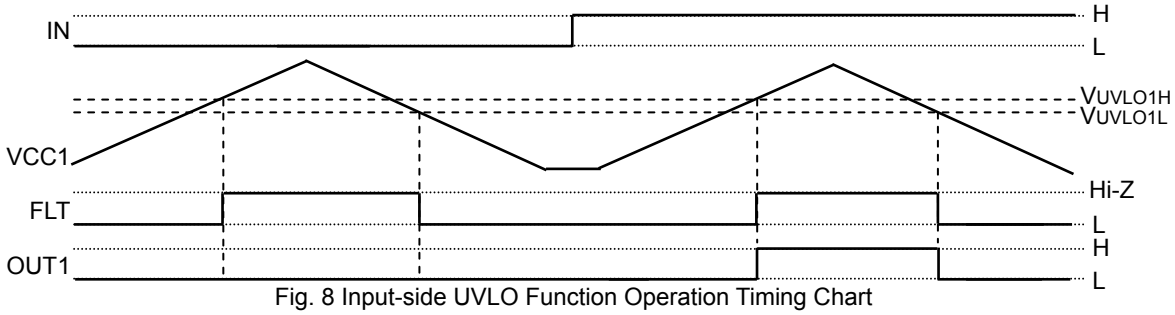


Fig. 8 Input-side UVLO Function Operation Timing Chart

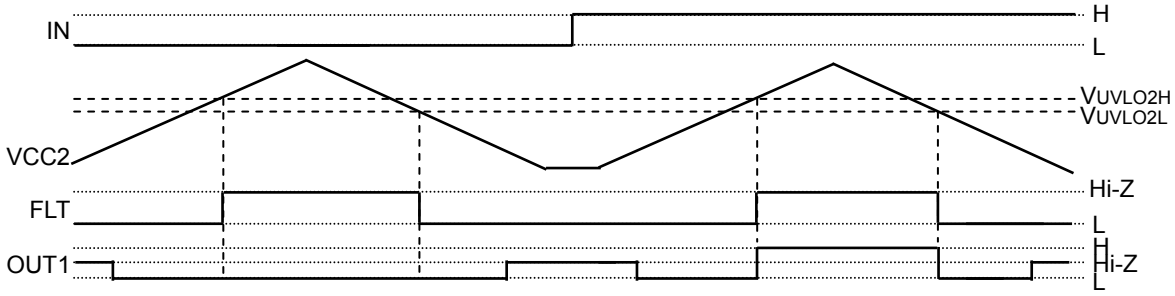


Fig. 9 Output-side UVLO Operation Timing Chart

4) Short current protection function (SCP, DESAT)

When the SCPIN pin voltage exceeds V_{SCDET}, the SCP function will be activated. When the SCP function is activated, the OUT1 pin voltage will be set to the “Hi-Z” level first, and then the PROOUT pin voltage to the “L” level (soft turn-off).Next, after t_{STO} has passed after the short-circuit current falls below the threshold value, OUT1pin becomes L and PROOUT pin becomes L. Finally, when the fault output holding time set in “2) fault status output” section on page 5 is completed, the SCP function will be released.

$V_{COLLECTOR}/V_{DRAIN}$ which Desaturation Protection starts operation (V_{DESAT}) and the blanking time (t_{BLANK}) can be calculated by the formula below;

$$V_{DESAT}[V] = V_{SCDET} \bullet \frac{R3+R2}{R3} - V_{F_{D1}}$$

$$V_{CC2_{MIN}}[V] > V_{SCDET} \bullet \frac{R3+R2+R1}{R3}$$

$$t_{BLANK\,outernal}[s] = -\frac{R2+R1}{R3+R2+R1} \bullet R3 \bullet C_{BLANK} \bullet ln(1 - \frac{R3+R2+R1}{R3} \bullet \frac{V_{SCDET}}{V_{CC2}}) + 0.2 \bullet 10^{-6}$$

V_{DESAT}	Reference Value		
	R1	R2	R3
4.0V	15 kΩ	39 kΩ	6.8 kΩ
4.5V	15 kΩ	43 kΩ	6.8 kΩ
5.0V	15 kΩ	36 kΩ	5.1 kΩ
5.5V	15 kΩ	39 kΩ	5.1 kΩ
6.0V	15 kΩ	43 kΩ	5.1 kΩ
6.5V	15 kΩ	62 kΩ	6.8 kΩ
7.0V	15 kΩ	68 kΩ	6.8 kΩ
7.5V	15 kΩ	82 kΩ	7.5 kΩ
8.0V	15 kΩ	91 kΩ	8.2 kΩ
8.5V	15 kΩ	82 kΩ	6.8 kΩ
9.0V	15 kΩ	130 kΩ	10 kΩ
9.5V	15 kΩ	91 kΩ	6.8 kΩ
10.0V	15 kΩ	130 kΩ	9.1 kΩ

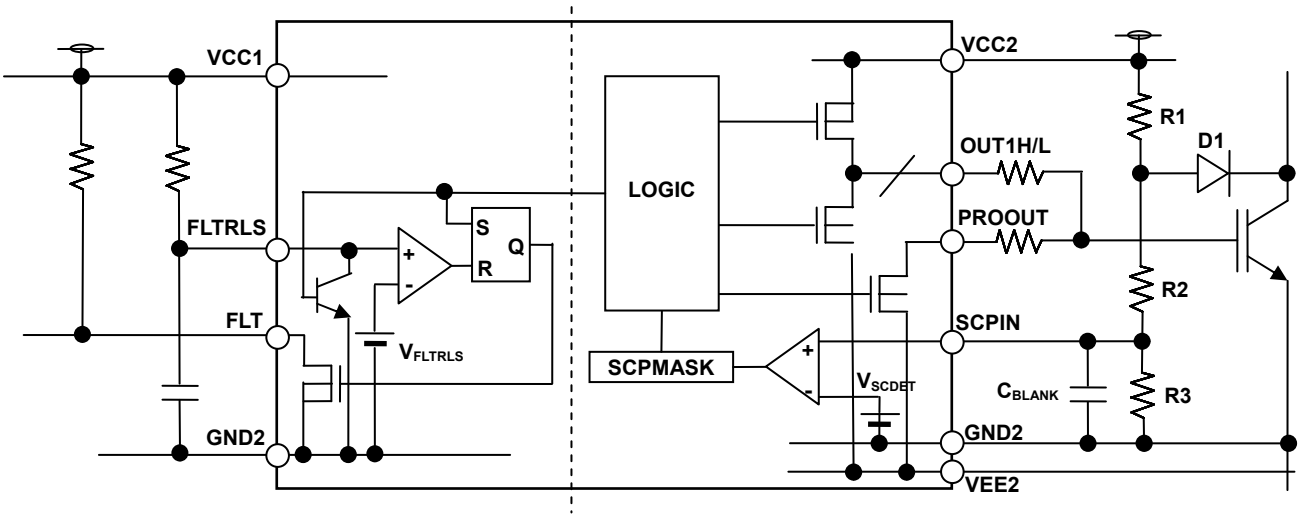
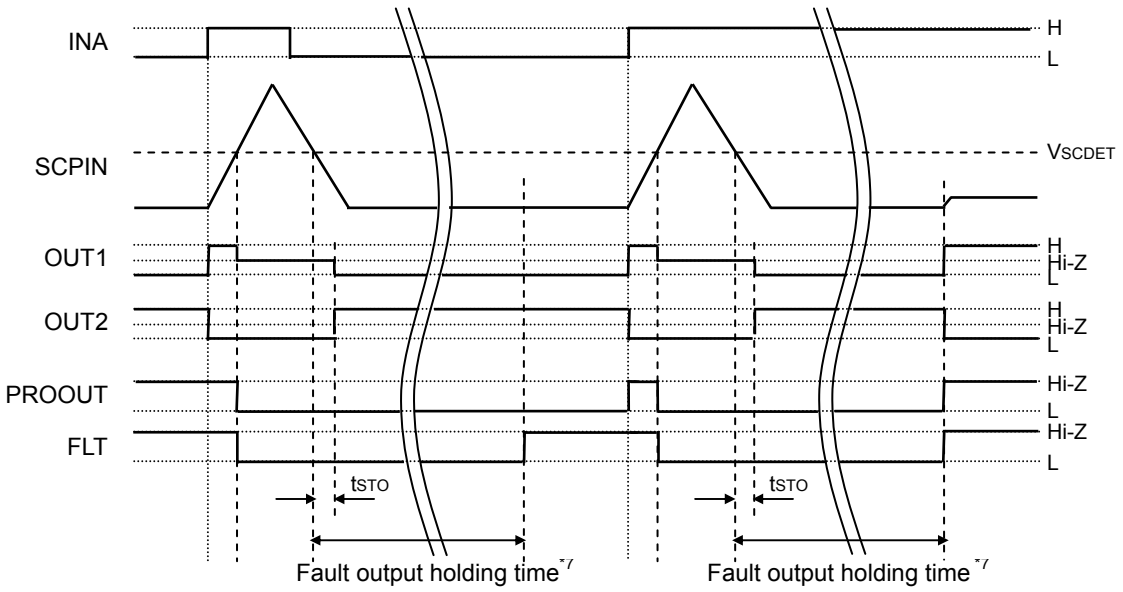


Fig. 10 Block Diagram for DESAT



*7: "2) Fault status output" section on page 5

Fig. 11 SCP (DESAT) Operation Timing Chart

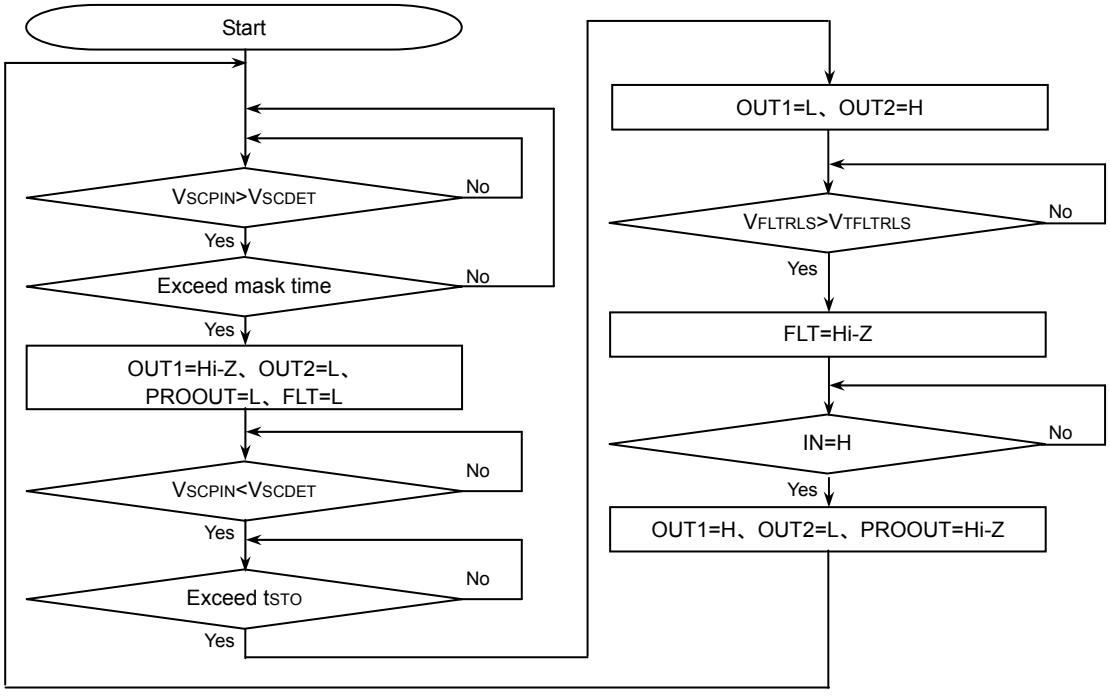


Fig. 12 SCP Operation Status Transition Diagram

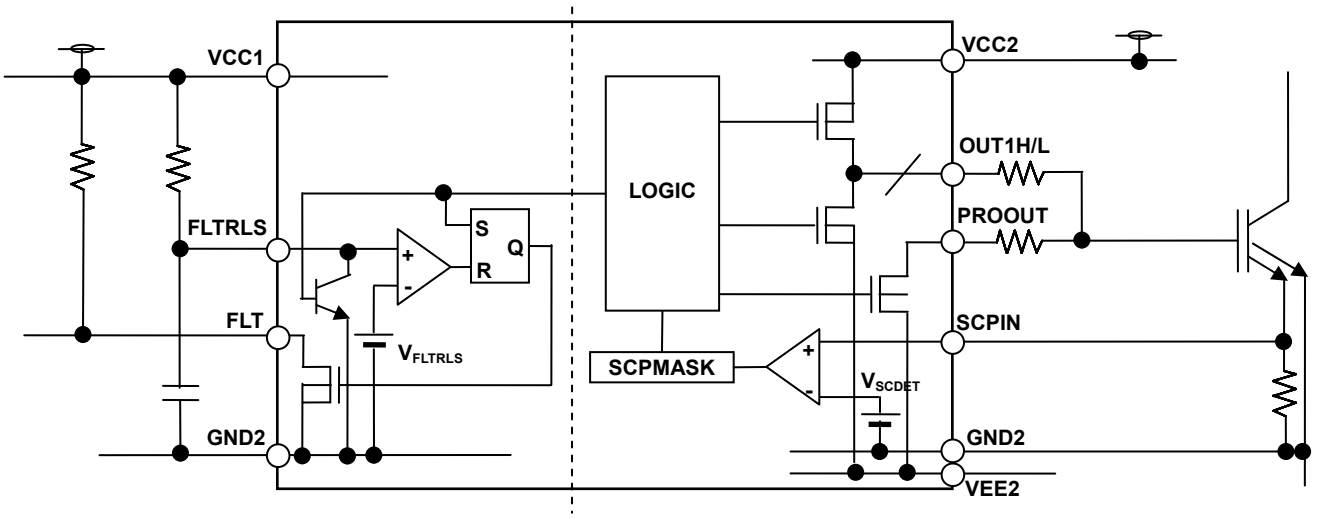


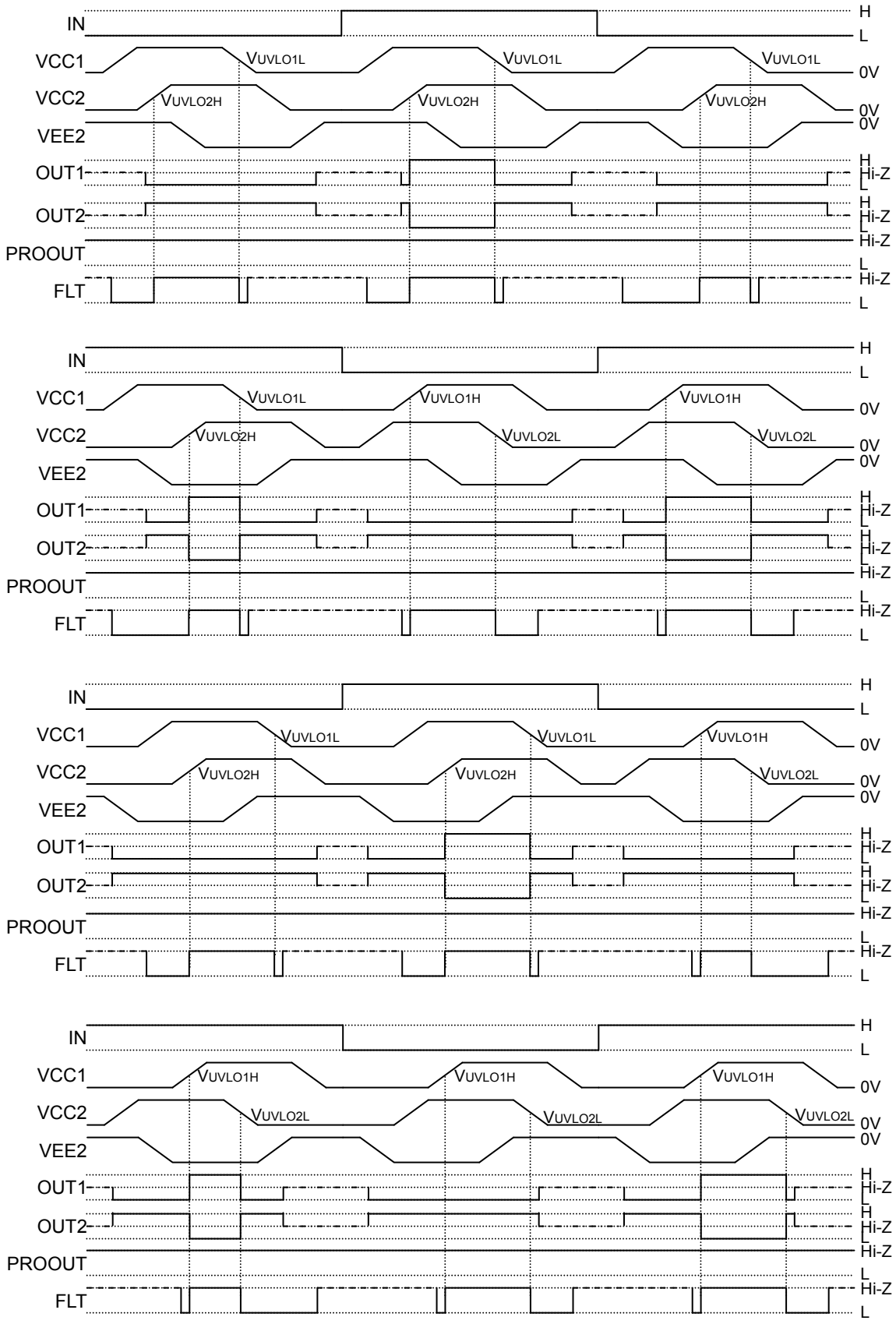
Fig. 13 Block Diagram for SCP

5）I/O condition table

No.	Status	Input							Output				
		VCC1	VCC2	SCPIN	ENA	INB	INA	PROOUT	OUT1	OUT2	PROOUT	FLT	OSFB
1	SCP	○	○	H	L	L	H	X	Hi-Z	L	L	L	Hi-Z
2	VCC1UVLO	UVLO	X	L	X	X	X	H	L	L	Hi-Z	L	Hi-Z
3		UVLO	X	L	X	X	X	L	L	H	Hi-Z	L	Hi-Z
4	VCC2UVLO	X	UVLO	L	X	X	X	H	L	L	Hi-Z	L	Hi-Z
5		X	UVLO	L	X	X	X	L	L	H	Hi-Z	L	Hi-Z
6	Disable	○	○	L	H	X	X	H	L	L	Hi-Z	Hi-Z	Hi-Z
7		○	○	L	H	X	X	L	L	H	Hi-Z	Hi-Z	Hi-Z
8	INB active	○	○	L	L	H	X	H	L	L	Hi-Z	Hi-Z	L
9		○	○	L	L	H	X	L	L	H	Hi-Z	Hi-Z	Hi-Z
10	Normal operation L input	○	○	L	L	L	L	H	L	L	Hi-Z	Hi-Z	L
11		○	○	L	L	L	L	L	L	H	Hi-Z	Hi-Z	Hi-Z
12	Normal operation H input	○	○	L	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z
13		○	○	L	L	L	H	L	H	L	Hi-Z	Hi-Z	L

○: VCC1 or VCC2 > UVLO, X:Don't care

6) Power supply startup / shutoff sequence



: Since the VCC2 to VEE2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

: Since the VCC1 pin voltage is low and the FLT output MOS does not turn ON, the output pins become Hi-Z conditions.

Fig.14 Power supply startup / shutoff sequence

●Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3～+7.0[*1]	V
Output-side positive supply voltage	V_{CC2}	-0.3～+30.0[*2]	V
Output-side negative supply voltage	V_{EE2}	-15.0～+0.3[*2]	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	36.0	V
INA, INB, ENA pin input voltage	V_{IN}	-0.3～+VCC1+0.3 or 7.0[*1]	V
OSFB, FLT pin input voltage	V_{FLT}	-0.3～+VCC1+0.3 or 7.0[*1]	V
FLTRLS pin input voltage	V_{FLTRLS}	-0.3～+VCC1+0.3 or 7.0[*1]	V
SCPIN pin input voltage	V_{SCPIN}	-0.3~VCC2+0.3[*2]	V
VREG pin output current	I_{VREG}	10	mA
OUT1H, OUT1L pin output current (DC)	I_{OUT1}	0.4[*3]	A
OUT1H, OUT1L pin output current (Peak 1us)	$I_{OUT1PEAK}$	5.0	A
OUT2 pin output current (DC)	I_{OUT2}	0.1[*3]	A
OUT2 pin output current (Peak 1us)	$I_{OUT2PEAK}$	1	A
PROOUT pin output current	I_{PROOUT}	0.2[*3]	A
OSFB output current	I_{OSFB}	10	mA
FLT output current	I_{FLT}	10	mA
Power dissipation	P_d	1.19[*4]	W
Operating temperature range	T_{opr}	-40～+125	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	+150	℃

*1 Relative to GND1.
*2 Relative to GND2.
*3 Should not exceed Pd and Tj=150°C.
*4 Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

●Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CC1}[*5]	4.5	5.5	V
Output-side positive supply voltage	V_{CC2}[*6]	14	24	V
Output-side negative supply voltage	V_{EE2}[*6]	-12	0	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	14	32	V

***5 Relative to GND1.**
***6 Relative to GND2.**

●Insulation related characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

●**Electrical Characteristics**

（Unless otherwise specified Ta=-40℃~125℃, V_{CC1}=4.5V~5.5V, V_{CC2}=UVLO_V_{CC2}~24V, V_{EE2}=-12V~0V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC1}	0.38	0.51	0.64	mA	OUT1=L
Input side circuit current 2	I_{CC12}	0.38	0.51	0.64	mA	OUT1=H
Input side circuit current 3	I_{CC13}	0.47	0.62	0.77	mA	INA=10kHz, Duty=50%
Input side circuit current 4	I_{CC14}	0.54	0.72	0.90	mA	INA=20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	1.5	2.0	2.5	mA	VCC2=14V, OUT1=L
Output side circuit current 2	I_{CC22}	1.3	1.8	2.3	mA	VCC2=14V, OUT1=H
Output side circuit current 3	I_{CC23}	1.6	2.2	2.8	mA	VCC2=18V, OUT1=L
Output side circuit current 4	I_{CC24}	1.3	1.9	2.5	mA	VCC2=18V, OUT1=H
Output side circuit current 5	I_{CC25}	1.8	2.5	3.2	mA	VCC2=24V, OUT1=L
Output side circuit current 6	I_{CC26}	1.5	2.1	2.7	mA	VCC2=24V, OUT1=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB, ENA
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB, ENA
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB
Logic pull-up resistance	R_{INU}	25	50	100	kΩ	ENA
Logic input mask time	t_{INMSKA}	-	-	90	ns	INA
	t_{INMSKB}	-	-	75	ns	INB
ENA mask time	t_{FLTMSK}	4	10	20	us	ENA
Output						
OUT1H ON resistance	R_{ONH}	0.7	1.8	4.0	Ω	I_{OUT1}=40mA
OUT1L ON resistance	R_{ONL}	0.4	0.9	2.0	Ω	I_{OUT1}=40mA
OUT1 maximum current	I_{OUTMAX}	3.0	4.5	-	A	VCC2=18V Guaranteed by design
PROOUT ON resistance	R_{ONPRO}	0.4	0.9	2.0	Ω	I_{PROOUT}=40mA
Turn ON time	t_{PON}	90	115	150	ns	
Turn OFF time	t_{POFF}	90	115	150	ns	
Propagation distortion	t_{PDIST}	-25	0	20	ns	t_{POFF} - t_{PON}
Rise time	t_{RISE}	-	50	100	ns	10nF between OUT1-VEE2
Fall time	t_{FALL}	-	50	100	ns	10nF between OUT1-VEE2
OUT2 ON resistance (Source)	R_{ON2H}	2.0	4.5	9.0	Ω	I_{OUT2}=40mA
OUT2 ON resistance (Sink)	R_{ON2L}	1.5	3.5	7.0	Ω	I_{OUT2}=40mA
OUT2 ON threshold voltage	V_{OUT2ON}	1.8	2	2.2	V	Relative to VEE2
OUT2 output delay time	t_{OUT2ON}	-	25	50	ns	
VREG output voltage	V_{REG}	9	10	11	V	Relative to VEE2
Common Mode Transient Immunity	CM	100	-	-	kV/us	design assurance

●**Electrical Characteristics**

（Unless otherwise specified Ta=-40℃~125℃, V_{CC1}=4.5V~5.5V, V_{CC2}=UVLO_V_{CC2}~24V, V_{EE2}=-12V~0V）

Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	4	10	30	us	
VCC2 UVLO OFF voltage	V_{UVLO2H}	9.10	9.55	10.00	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	8.60	9.05	9.50	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	4	10	30	us	
SCPIN Input voltage	V_{SCPIN}	-	0.1	0.22	V	I_{SCPIN}=1mA
SCP threshold voltage	V_{SCDET}	0.665	0.700	0.735	V	
SCP detection mask time	t_{SCPMSK}	0.55	0.8	1.05	us	
Soft turn OFF release time	t_{STO}	30		110	us	
OSFB threshold voltage H	V_{OSFBH}	4.5	5.0	5.5	V	Respective to GND2
OSFB threshold voltage L	V_{OSFBL}	4.0	4.5	5.0	V	Respective to GND2
OSFB output low voltage	V_{OSFBL}	-	0.18	0.40	V	I_{OSFB}=5mA
OSFB filter time	t_{OSFBON}	1.5	2.0	2.6	us	
FLT output low voltage	V_{FLTL}	-	0.18	0.40	V	I_{FLT}=5mA
FLTRLS threshold	$V_{TFLTRLS}$	$0.64 \times V_{CC1}$ -0.1	$0.64 \times V_{CC1}$	$0.64 \times V_{CC1}$ +0.1	V	

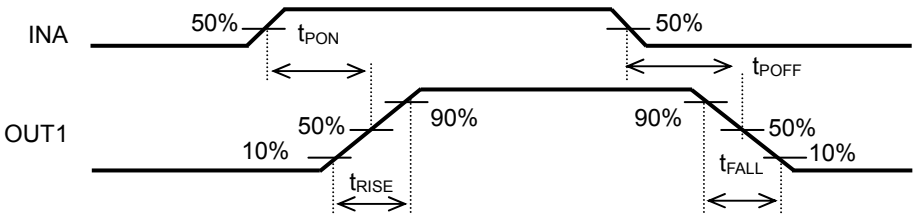


Fig.15 INA-OUT1 Timing Chart

●Typical Performance Curves

T.B.D.

Fig.16 – Fig.60

●**Selection of Components Externally Connected**

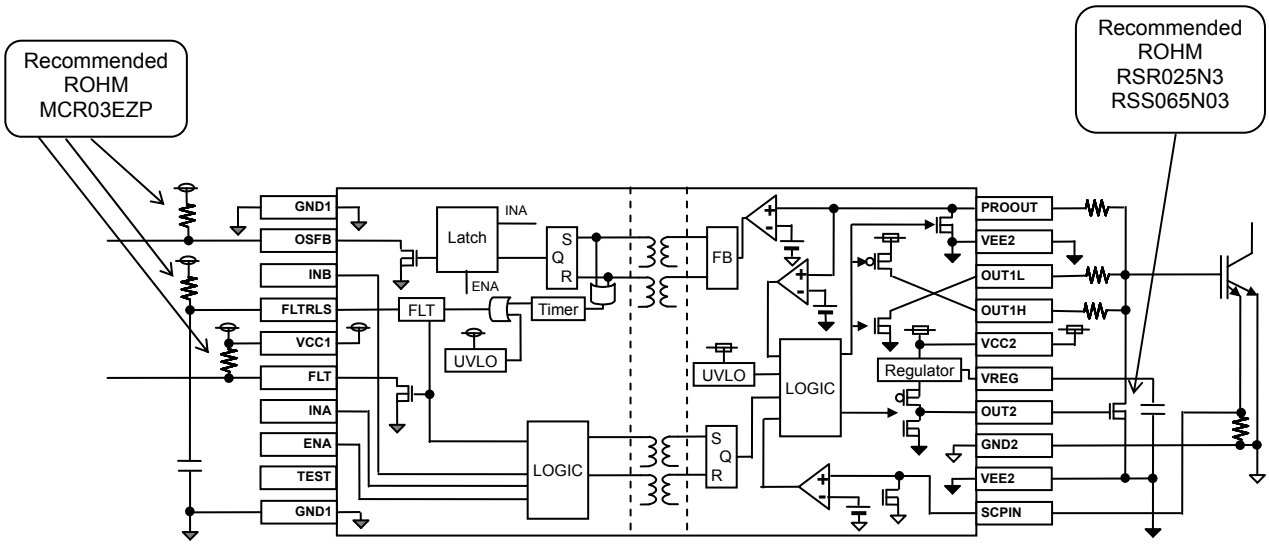


Fig.61 For using 4-pin IGBT (for using SCP function)

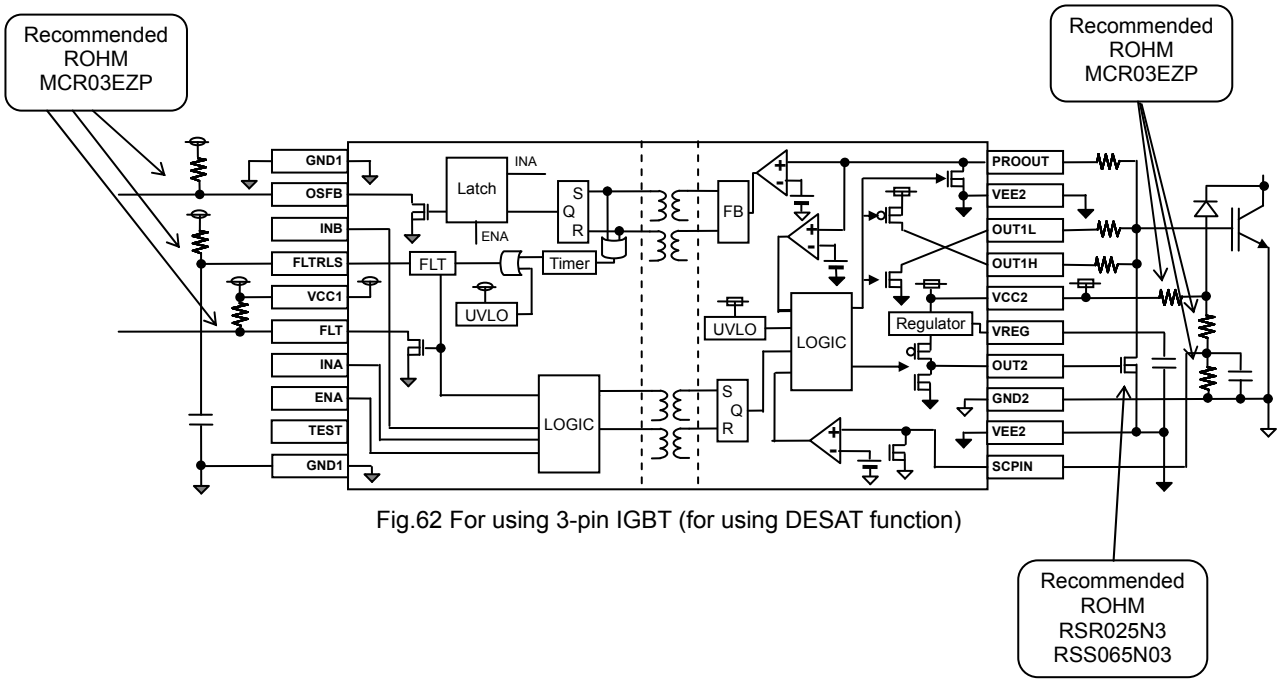


Fig.62 For using 3-pin IGBT (for using DESAT function)

●**Power Dissipation**

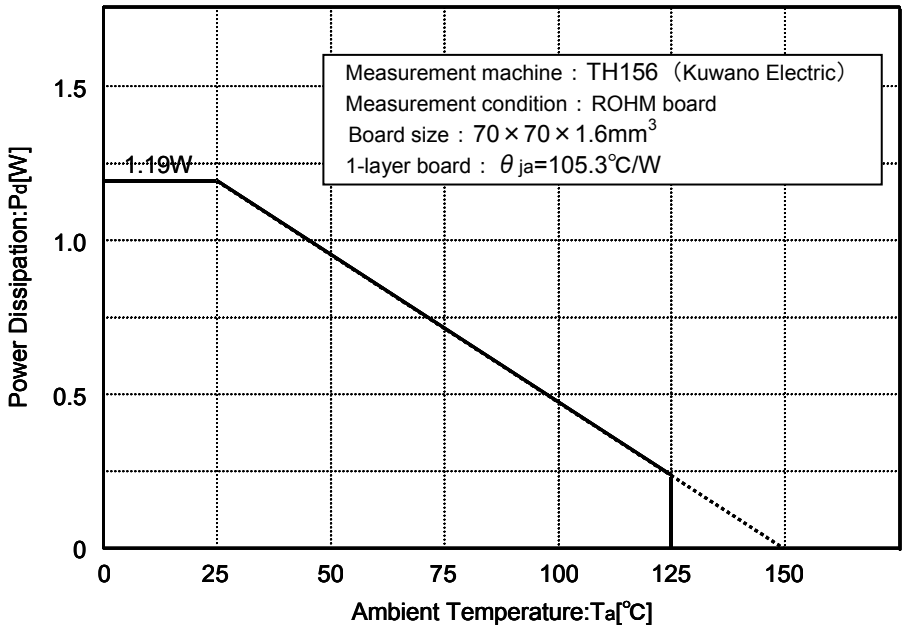
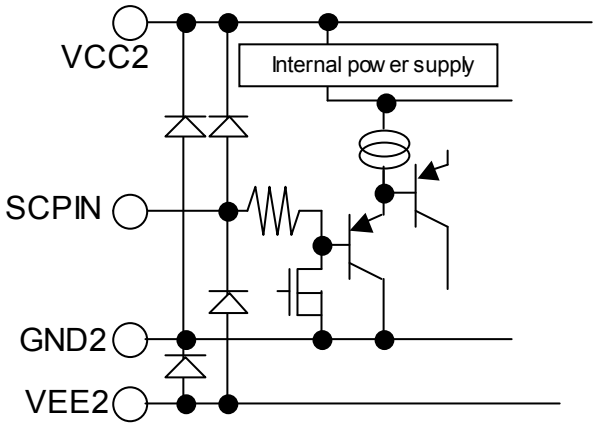
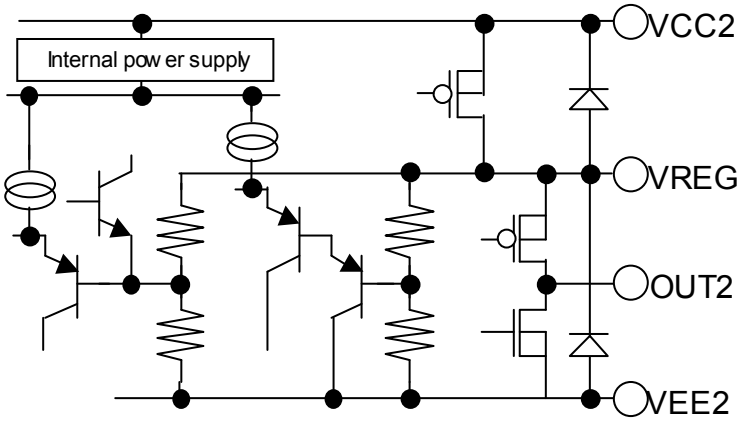
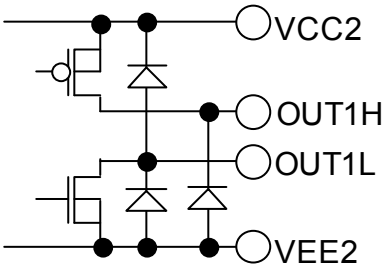
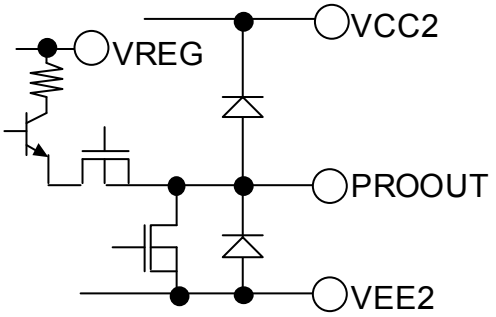


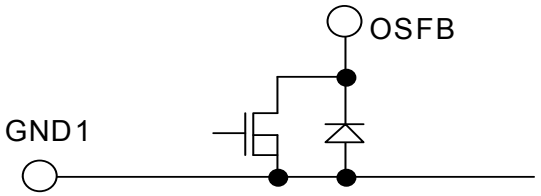
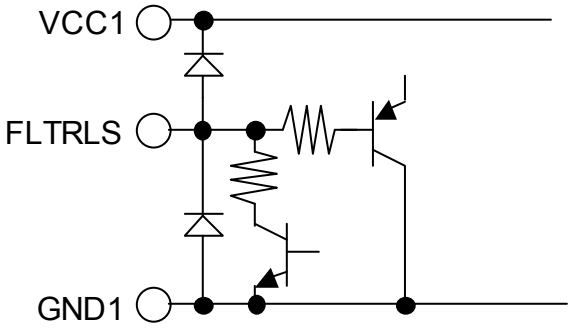
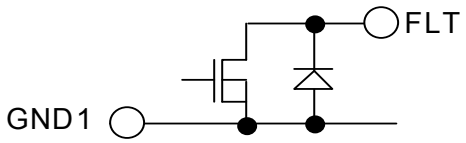
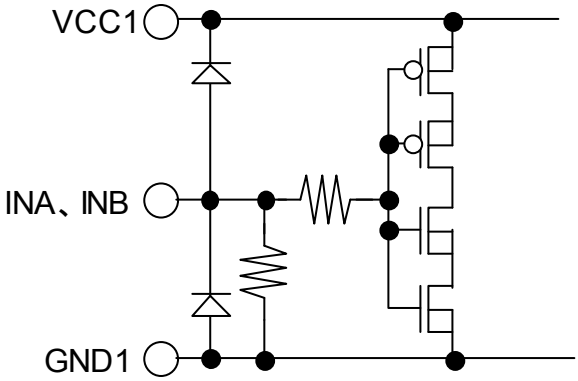
Fig.63 SSOP-B20W Derating Curve

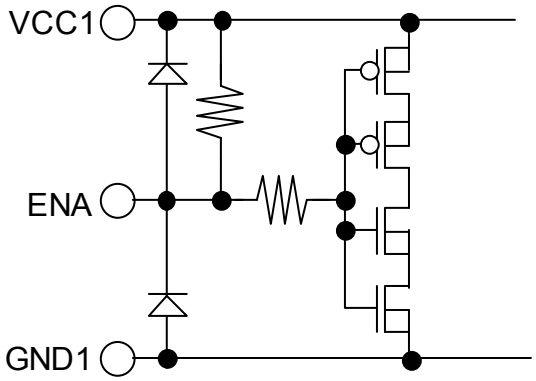
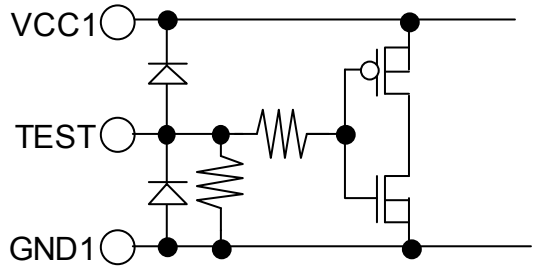
●**Thermal design**

Please confirm that the IC's chip temperature Tj is not over 150℃, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150℃ is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150℃ must be strictly obeyed under all circumstances.

●I/O equivalence circuits

Pin No.	Name / Function	I/O equivalence circuits
1	SCPIN Short current detection pin	
4	OUT2 MOS FET control pin for Miller Clamp	
5	VREG Power supply pin for driving MOS FET for Miller Clamp	
7	OUT1H Source side output pin	
8	OUT1L Sink side output pin	
10	PROOUT Soft turn-off pin	

Pin No.	Name / Function	I/O equivalence circuits
12	OSFB Output state feedback pin	
14	FLTRLS Fault output holding time setting pin	
16	FLT Fault output pin	
13 17	INB Opposite driver's control input pin INA Control input pin	

Pin No.	Name / Function	I/O equivalence circuits
18	ENA Input enabling signal input pin	
19	TEST Test mode setting pin	

●Operational Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND1 Potential

The potential of GND1 pin must be minimum potential in all operating conditions. (Input side ; 11pin to 20pin)

(5) VEE2 Potential

The potential of VEE2 pin must be minimum potential in all operating conditions. (Output side ; 1pin to 10pin)

(6) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(7) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(8) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(9) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(10) Input terminal of IC

Between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.

For example, when the resistance and transistor are connected to the terminal as shown in figure 21,

- ○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
- ○Also, when GND＞(Terminal B) at the transistor (NPN), The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

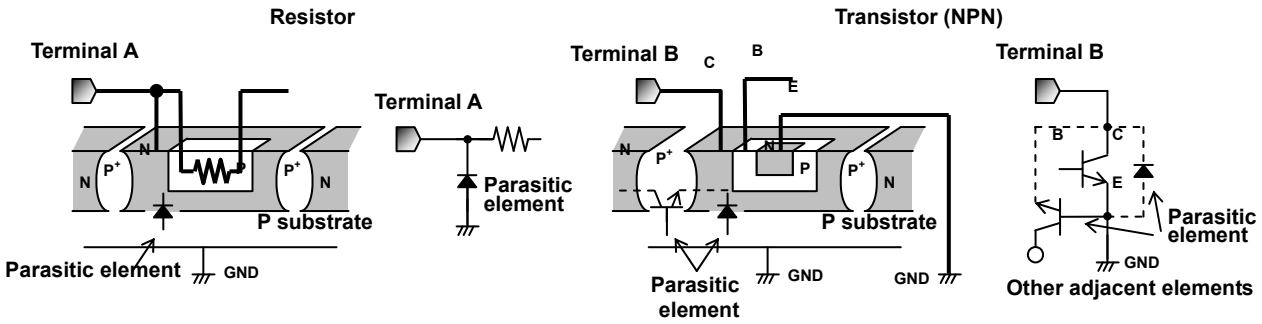


Fig.64 Pattern Diagram of Parasitic Element

(11) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

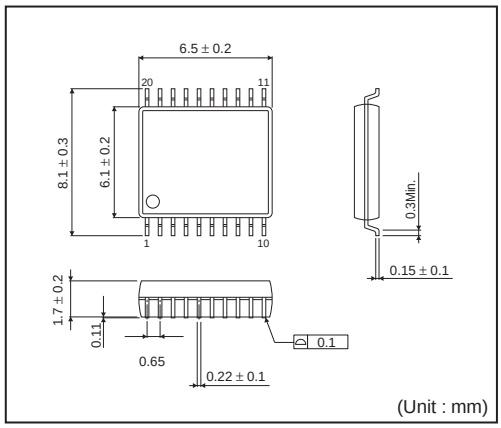
If there are any differences in translation version of this document formal version takes priority

●Ordering Information

B M 6 1 0 4 F V	-	CE 2
Part Number	Package FV:SSOP-B20W	Packaging and forming specification E2: Embossed tape and reel

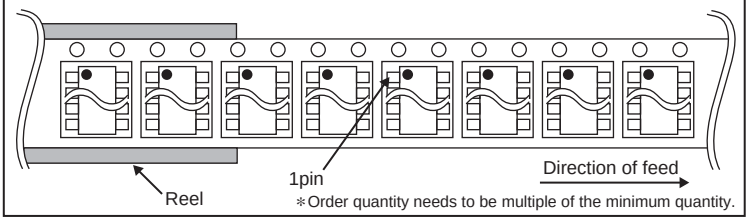
●Physical Dimension Tape and Reel Information

SSOP-B20W



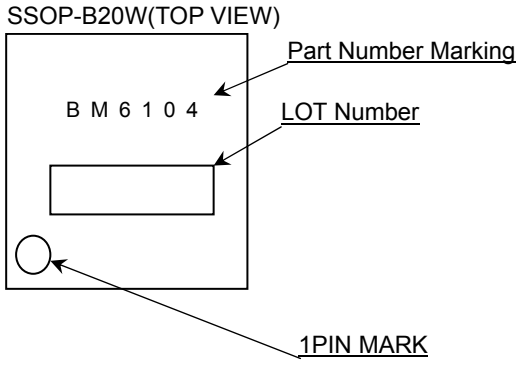
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)



●**Revision History**

Date	Revision	Changes	
19.Mar.2012	001	New Release	
10.Apr.2012	002	-	Changed the function of the OSFB pin, the FLT pin, and the INB pin
		-	Deleted the SCPTH pin
		-	Added the OUT1L pin (the name of OUT1 pin was changed to OUT1H)
18.Jun.2012	003	Page 1	Change General Description.
		Page 2	Change Pin Description 'OUT2, VREG pin'.
		Page 3	Change Description of pins and cautions on layout of board 'OUT2, VREG, PROOUT pin'.
		Page 4	Change Description of pins and cautions on layout of board 'OSFB pin'.
		Page 4	Change Description of functions and example of constant setting '1)'.
		Page 5	Change Description of functions and example of constant setting '2) '.
		Page 6	Change Description of functions and example of constant setting'4)' Equation of $t_{BLANKouternal}$.
		Page 11	Delete Absolute Maximum Rating 'Output-side ground potential' .
		Page 11	Add Insulation related characteristics.
		Page 12	Delete Electrical Characteristics 'OSFB output low hold time' .
		Page 12	Add Electrical Characteristics 'Common Mode Transient Immunity' .
		Page 12	Change Electrical Characteristics 'SCP threshold voltage' .
		Page 25	Delete Recommended Part Number 'RHK005N03'.
		Page 27	Change Function of I/O equivalence circuit 'OUT2, VREG pin' .
		Page 30	Change Operation Note '(4) and (5)'.
23.Jul.2012	**004**	Page 1	Change I/O delay time
			Change Minimum input pulse width
		Page 8	Change 'I/O condition table'
		Page 11	Change Electrical Characteristics 'Logic input mask time'
			Change Electrical Characteristics 'Turn ON time'
			Change Electrical Characteristics 'Turn OFF time'
			Change Electrical Characteristics 'Propagation distortion'
9.Oct.2012	**005**	Page 1	Change 'Fig.1', 'Fig.2'
		Page 8	Change 'I/O condition table'
		Page 11	Change Electrical Characteristics 'Output side circuit current'
			Change Electrical Characteristics 'Logic input mask time'
			Change Electrical Characteristics 'Turn ON time'
			Change Electrical Characteristics 'Turn OFF time'
			Change Electrical Characteristics 'Propagation distortion'
			Change Electrical Characteristics 'OUT2 output delay time'
		Page 12	Change Electrical Characteristics 'OSFB threshold voltage'
			Change Electrical Characteristics 'OSFB filter time'
		Page 14	Change 'Fig.61', 'Fig.62'
31.Jan.2013	**006**	Page 1	Change General Description
			Change Key Specifications 'Minimum input pulse width'
		Page 11	Change Electrical Characteristics 'Turn ON time'
			Change Electrical Characteristics 'Turn OFF time'
		Page 12	Change Electrical Characteristics 'VCC2 UVLO OFF voltage'
			Change Electrical Characteristics 'VCC2 UVLO ON voltage'
			Change Electrical Characteristics 'OSFB threshold voltage H'
			Change Electrical Characteristics 'OSFB filter time'
		Page 16	Change I/O equivalence circuits 'OUT1L'
10.Apr.2013	**007**	Page 8	Change 'I/O condition table'
		Page 11	Change Electrical Characteristics 'Input side circuit current'
			Change Electrical Characteristics 'Output side circuit current'
		Page 11,12	Change Electrical Characteristics condition of V_{CC2}.
		-	Change misprint from 'V_{SCPTH}' to 'V_{SCDET}'