Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM60014FV-C

●General Description

The BM60014FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 120ns, and minimum input pulse width of 70ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function and Miller clamp function.

●Key Specifications

- ■Isolation voltage: 2500[Vrms](Min.)
- ■Maximum gate drive voltage: 24[V](Max.)
- ■I/O delay time: 120[ns](Max.)
- ■Minimum input pulse width: 70[ns](Max.)

●Features

- ■ Providing Galvanic Isolation
- ■ Active Miller Clamping
- ■ Fault signal output function
- ■ Undervoltage lockout function

●Package

SSOP-B20W

W(Typ.) x D(Typ.) x H(Max.)
6.50mm x 8.10mm x 2.01mm

●Applications

- ■ Driving IGBT Gate
- ■ Driving MOSFET Gate

●Typical Application Circuits

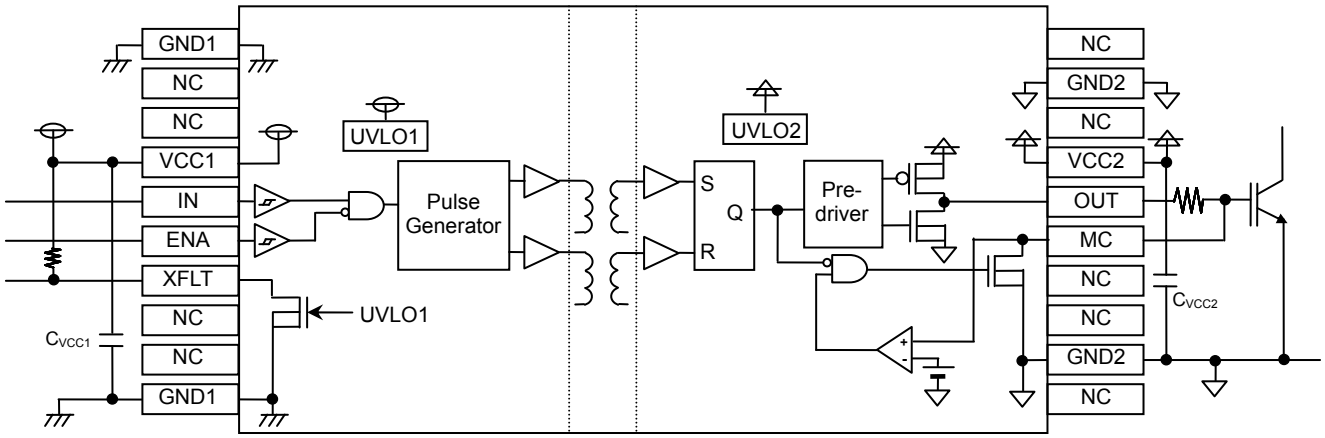


Figure 1. Application circuits

●**Recommended range of external constants**

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
VCC1	C_{VCC1}	0.1	1.0	-	μF
VCC2	C_{VCC2}	0.33	-	-	μF

●**Pin Configurations**

SSOP-B20W
(TOP VIEW)

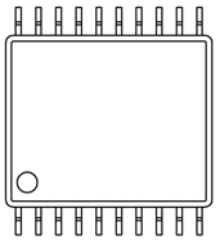


Figure 2. Pin configuration

●**Pin Descriptions**

Pin No.	Pin Name	Function
1	NC	No Connect
2	GND2	Output-side ground pin
3	NC	No Connect
4	NC	No Connect
5	MC	Output pin for Miller Clamp
6	OUT	Output pin
7	VCC2	Output-side power supply pin
8	NC	No Connect
9	GND2	Output-side ground pin
10	NC	No Connect
11	GND1	Input-side ground pin
12	NC	No Connect
13	NC	No Connect
14	VCC1	Input-side power supply pin
15	IN	Control input pin
16	ENA	Input enabling signal input pin
17	XFLT	Fault signal output pin
18	NC	No Connect
19	NC	No Connect
20	GND1	Input-side ground pin

●Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side positive power supply pin)
The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side.

5) IN, ENA (Control input terminal)
The IN pin and the ENA pin are pins used to determine output logic.

ENA	IN	OUT
H	X	L
L	L	L
L	H	H

6) OUT (Output pin)
The OUT pin is a pin used to drive the gate of a power device.

7) MC (Output pin for Miller Clamp)
The MC pin is a pin for preventing increase in gate voltage due to the Miller current of the power device connected to OUT pin. If the Miller Clamp function is not used, short-circuit the MC pin to the GND2 pin.

8) XFLT (Fault signal output pin)
The FLT pin is an open drain pin used to output a fault signal at the input-side undervoltage lockout function (UVLO1).

Conditions	XFLT
While in normal operation	L
When an Fault occurs (When UVLO1 is activated)	Hi-Z

●**Description of functions and examples of constant setting**

1) Miller Clamp function

When IN=L and OUT pin voltage < V_{MCON}, the internal MOSFET of the MC pin is turned ON.

IN	MC	The internal MOSFET of the MC pin
L	less than V_{MCON}	ON
H	X	OFF

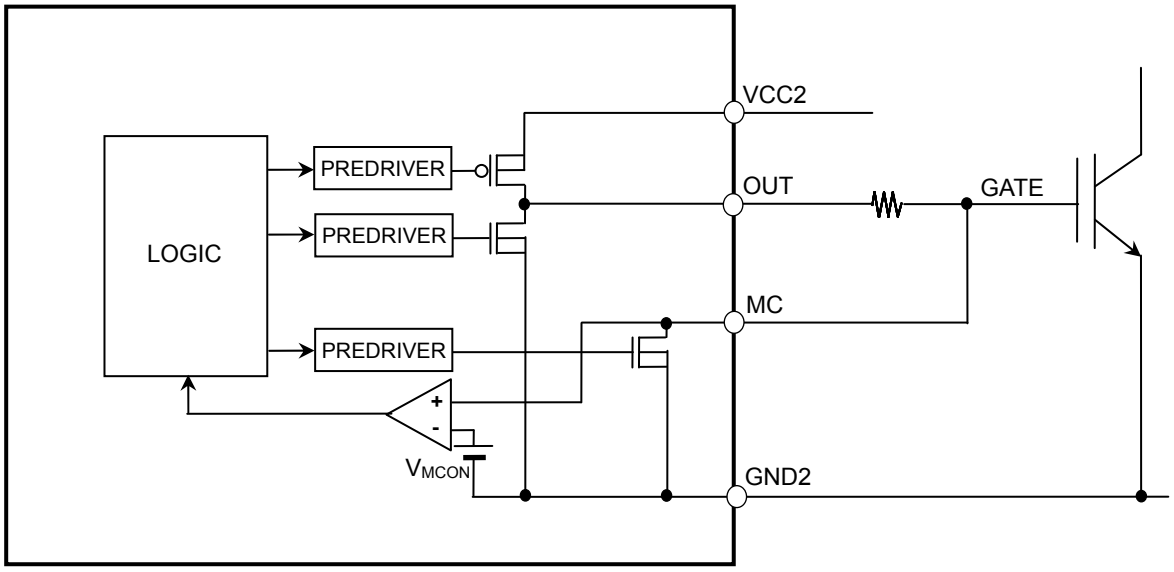


Figure 3. Block diagram of Miller Clamp function.

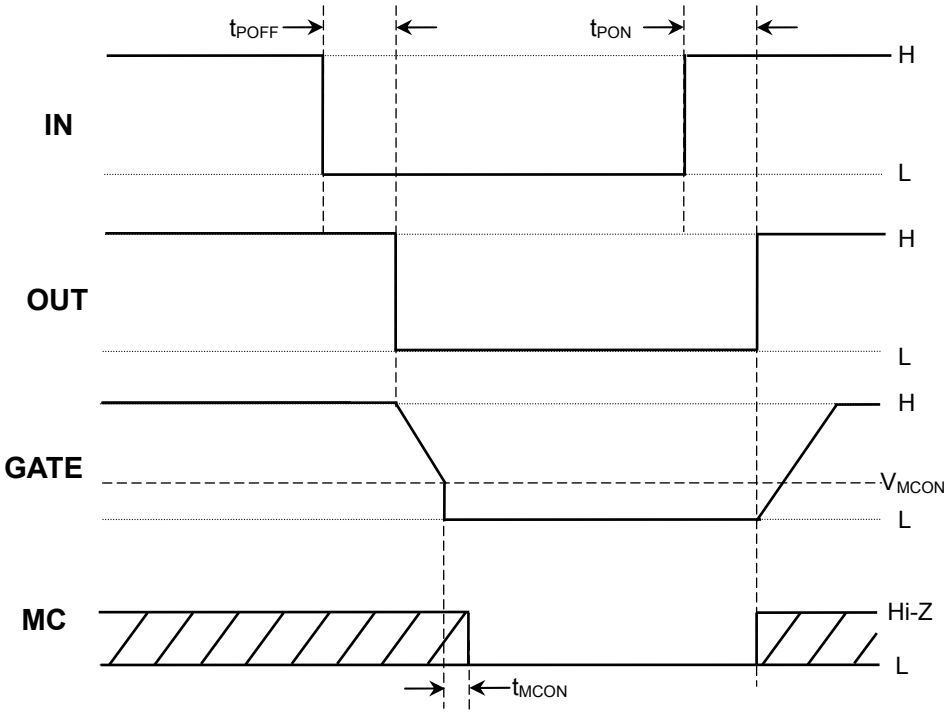


Figure 4. Timing chart of Miller Clamp function

2) Undervoltage Lockout (UVLO) function

The BM60014FV-C incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage, the OUT pin will output the “L” signal. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both low and high voltage sides.

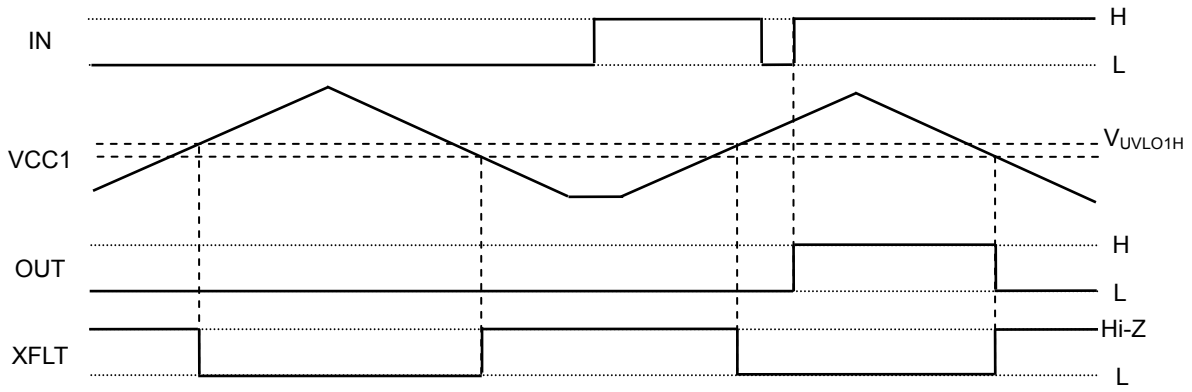


Figure 5. Input-side UVLO Function Operation Timing Chart

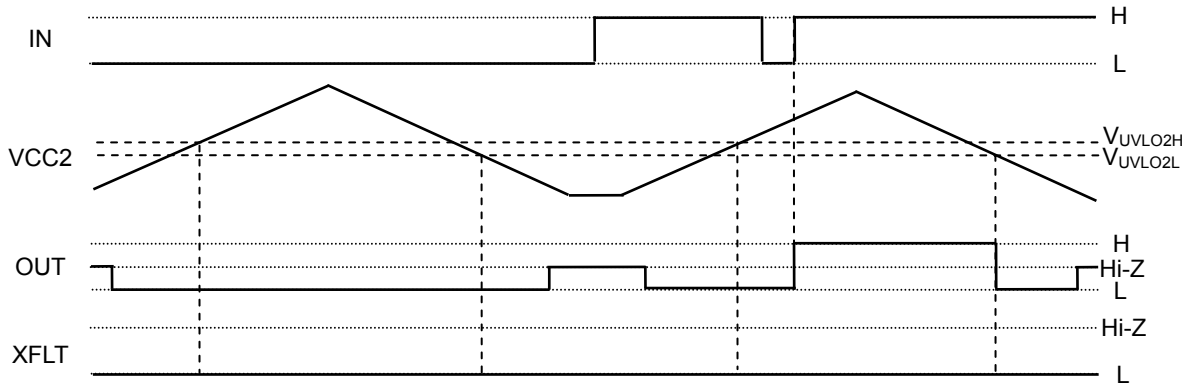


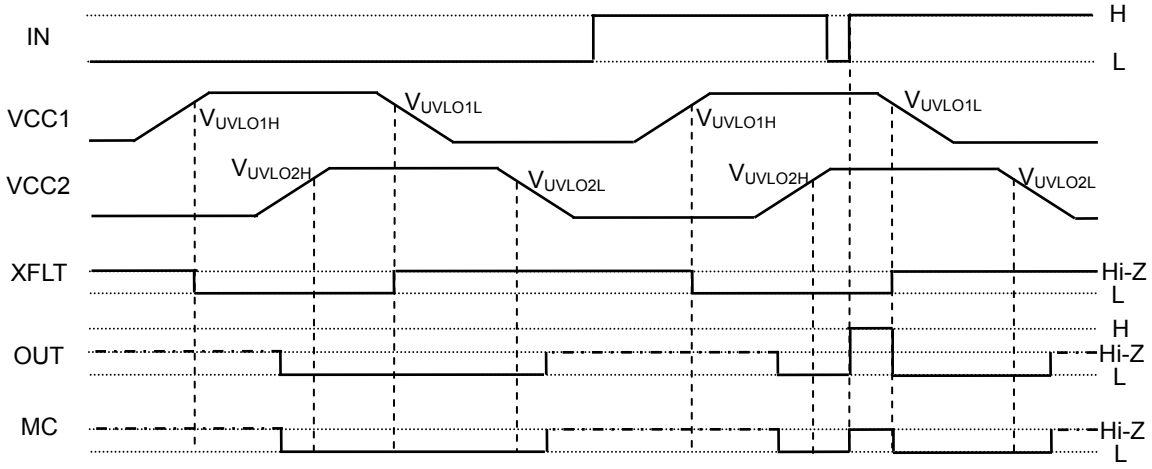
Figure 6. Output-side UVLO Function Operation Timing Chart

3）I/O condition table

No.	Status	Input				Output		
		VCC1	VCC2	ENA	IN	OUT	MC	XFLT
1	VCC1UVLO	UVLO	X	X	X	L	L	H
2	VCC2UVLO	X	UVLO	X	X	L	L	L
3	Disable	○	○	H	X	L	L	L
4	Normal operation L input	○	○	L	L	L	L	L
5	Normal operation H input	○	○	L	H	H	Hi-Z	L

○: VCC1 or VCC2 > UVLO, X:Don't care

4) Power supply startup / shutoff sequence



- - - - - - : Since the VCC2 to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 7. Power supply startup / shutoff sequence

●Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3～+7.0*1	V
Output-side supply voltage	V_{CC2}	-0.3～+30.0*2	V
IN pin input voltage	V_{IN}	-0.3～+VCC1+0.3 or +7.0*1	V
OUT pin output current	I_{OUT}	400*3	mA
OUT pin output current (Peak 10μs)	$I_{OUTPEAK}$	5000*3	mA
MC pin output current	I_{MC}	400*3	mA
XFLT pin output current	I_{XFLT}	10	mA
Power dissipation	P_d	1.19*4	W
Operating temperature range	T_{opr}	-40～+125	°C
Storage temperature range	T_{stg}	-55～+150	°C
Junction temperature	T_{jmax}	+150	°C

*1 Relative to GND1.
*2 Relative to GND2.
*3 Should not exceed Pd and Tj=150°C
*4 Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70mm ×70mm ×1.6mm.

●Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CC1}*5	4.5	5.5	V
Output-side supply voltage	V_{CC2}*6	10.0	24.0	V

*5 Relative to GND1.
*6 Relative to GND2.

●Insulation related characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

●Electrical Characteristics

（Unless otherwise specified Ta=-40°C ~125°C, V_{CC1}=4.5V~5.5V, V_{CC2}=10V ~ 24V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.06	0.14	0.22	mA	
Input side circuit current 2	I_{CC12}	0.10	0.20	0.30	mA	IN =10kHz, Duty=50%
Input side circuit current 3	I_{CC13}	0.15	0.30	0.45	mA	IN =20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	0.23	0.38	0.53	mA	OUT=L
Output side circuit current 2	I_{CC22}	0.20	0.34	0.48	mA	OUT=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	IN、ENA
Logic low level input voltage	V_{INL}	0	-	0.8	V	IN、ENA
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	IN、ENA
Logic input minimum pulse width	t_{INMin}	-	-	70	ns	IN、ENA
Output						
OUT ON resistance (Source)	R_{ONH}	0.4	0.9	2.0	Ω	I_{OUT}=-40mA
OUT ON resistance (Sink)	R_{ONL}	0.2	0.6	1.3	Ω	I_{OUT}=40mA
OUT maximum current (Source)	$I_{OUTMAXH}$	3.0	4.5	-	A	VCC2=15V, Guaranteed by design
OUT maximum current (Sink)	$I_{OUTMAXL}$	3.0	3.9	-	A	VCC2=15V, Guaranteed by design
Turn ON time	t_{PON}	70	90	120	ns	No load between OUT-GND2
Turn OFF time	t_{POFF}	70	90	120	ns	No load between OUT-GND2
Propagation distortion	t_{PDIST}	-20	0	20	ns	$t_{POFF} - t_{PON}$
Rise time	t_{RISE}	25	50	100	ns	10nF between OUT-GND2
Fall time	t_{FALL}	25	50	100	ns	10nF between OUT-GND2
MC ON resistance	R_{ONMC}	0.20	0.65	1.40	Ω	I_{MC}=40mA
MC ON threshold voltage	V_{MCON}	1.8	2	2.2	V	
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Guaranteed by design
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	1.0	2.5	5.0	μs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	9.0	9.5	10.0	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	8.0	8.5	9.0	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	1.00	2.85	5.00	μs	
XFLT output L voltage	V_{XFLT}	-	0.10	0.25	V	I_{XFLT}=5mA

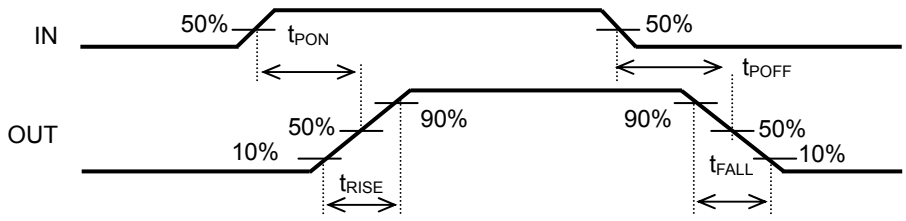


Figure 8. IN-OUT Timing Chart

●**Typical Performance Curves**

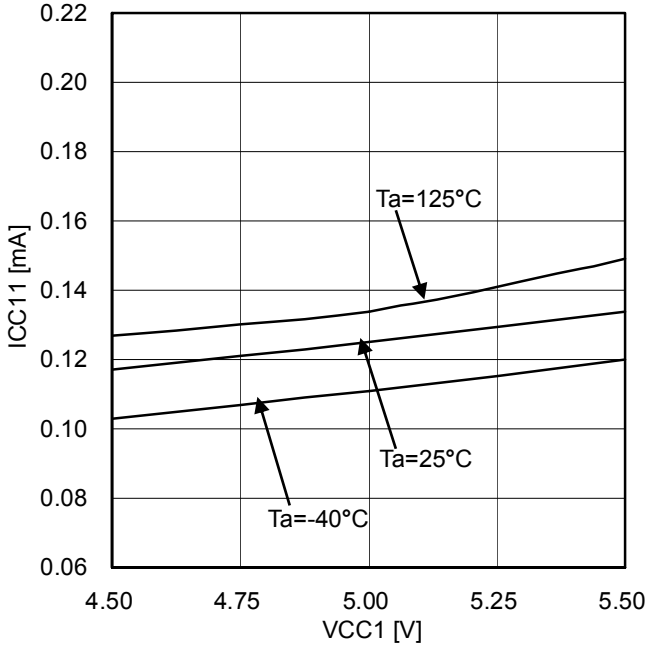


Figure 9. Input side circuit current

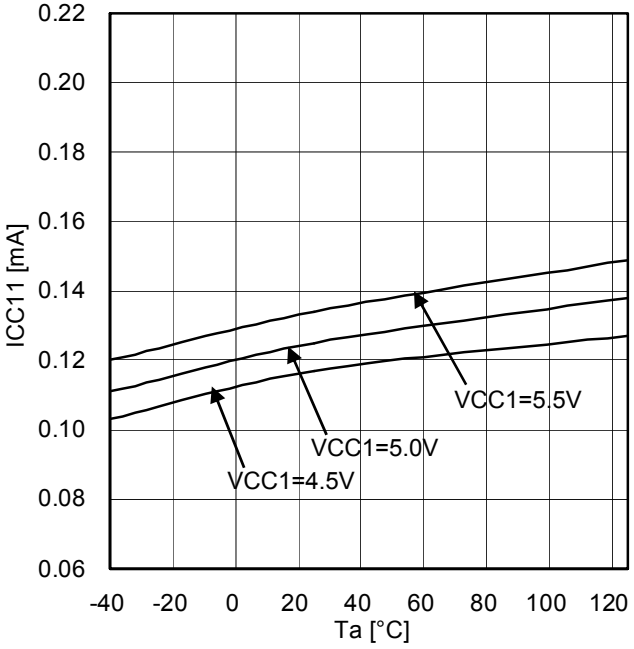


Figure 10. Input side circuit current

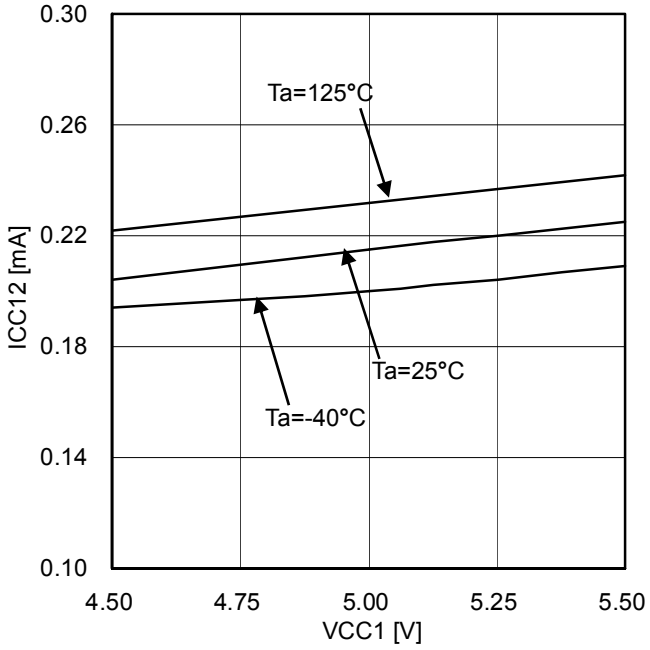


Figure 11. Input side circuit current
（at IN=10kHz, Duty=50%）

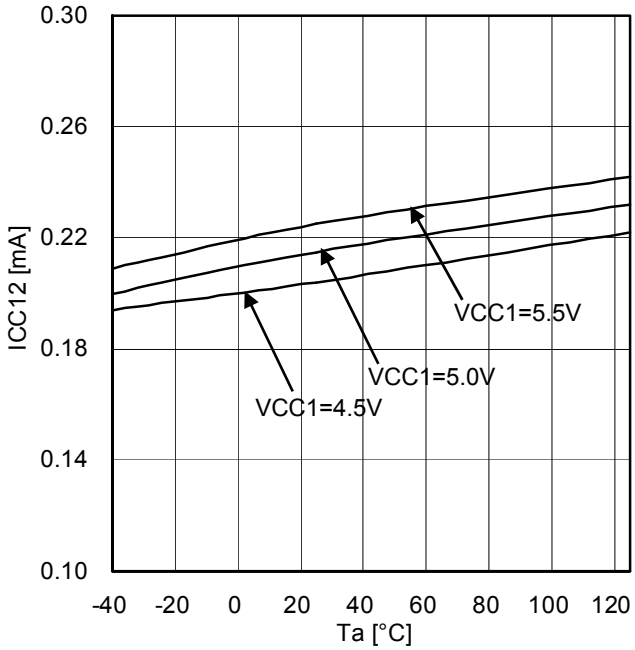


Figure 12. Input side circuit current
（at IN=10kHz, Duty=50%）

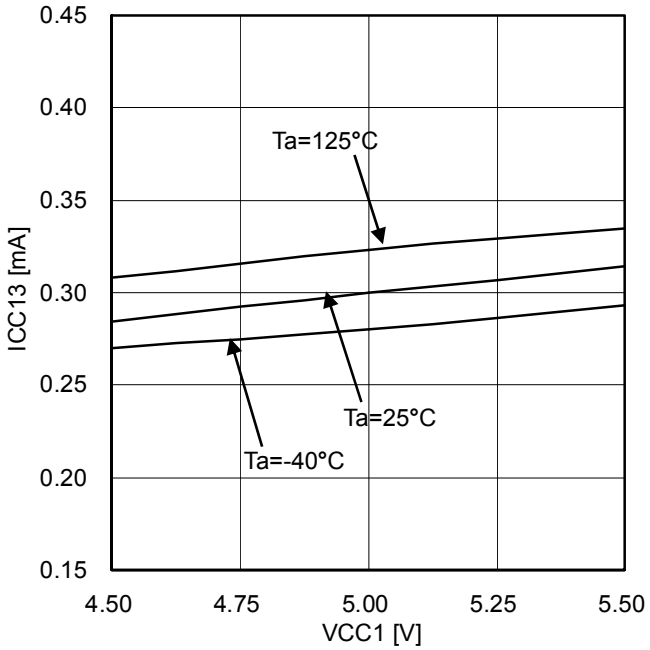


Figure 13. Input side circuit current
（at IN=20kHz, Duty=50%）

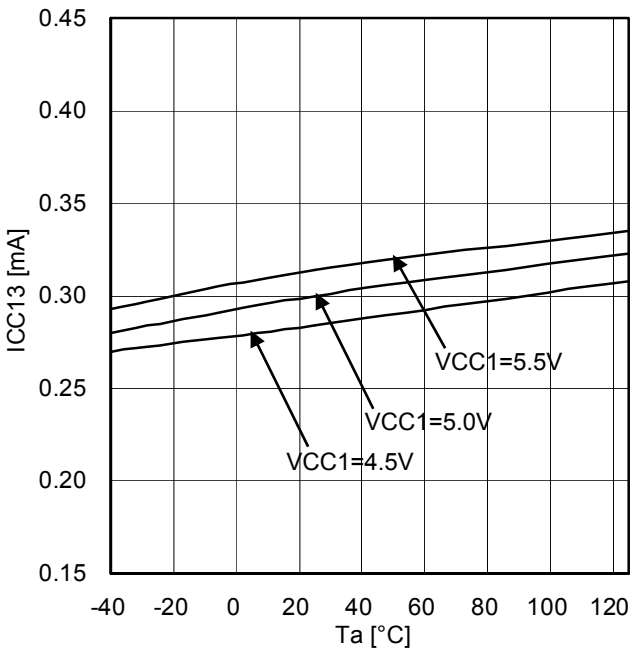


Figure 14. Input side circuit current
（at IN=20kHz, Duty=50%）

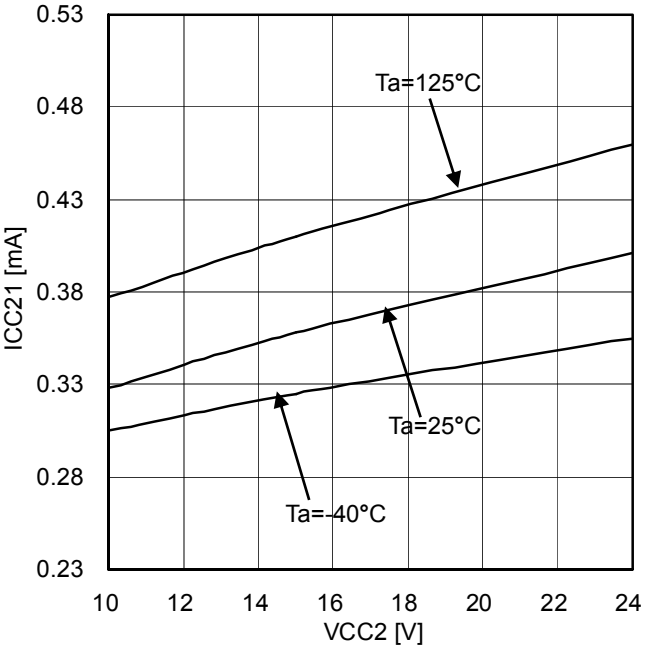


Figure 15. Output side circuit current（at OUT=L）

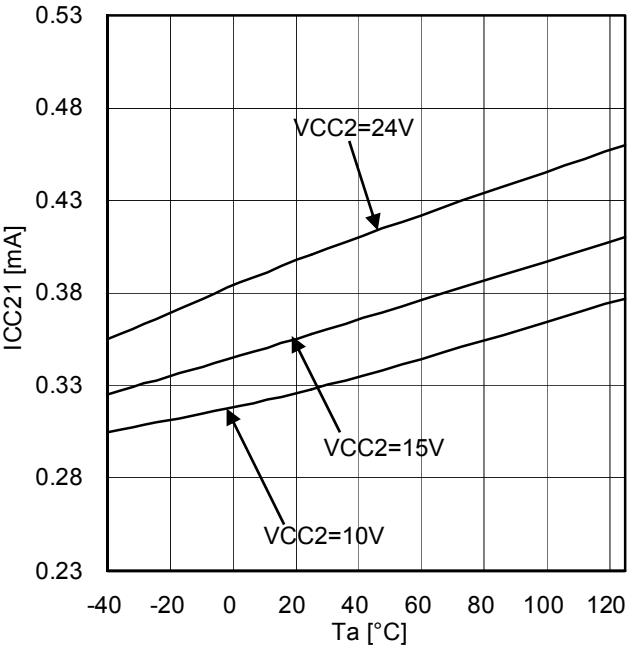


Figure 16. Output side circuit current（at OUT=L）

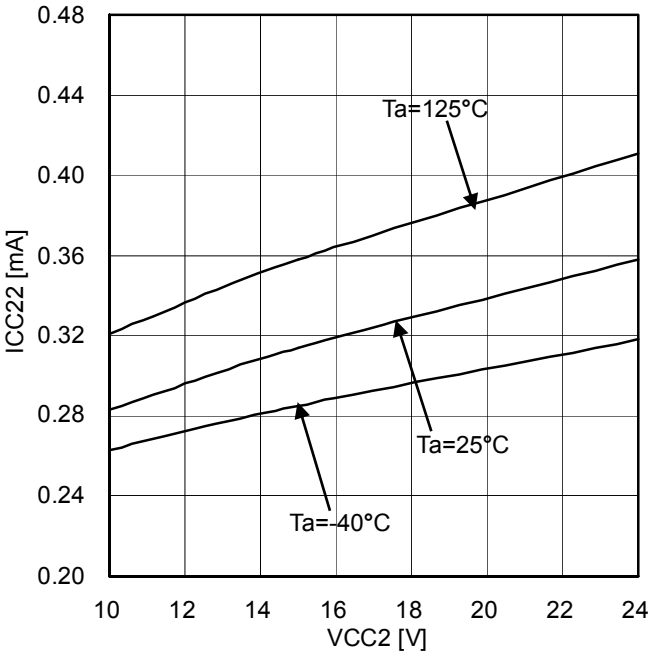


Figure 17. Output side circuit current（at OUT=H）

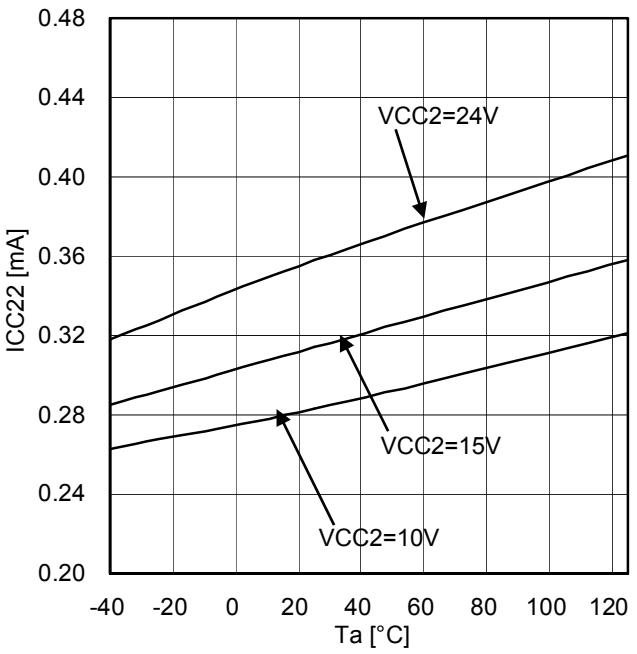


Figure 18. Output side circuit current（at OUT=H）

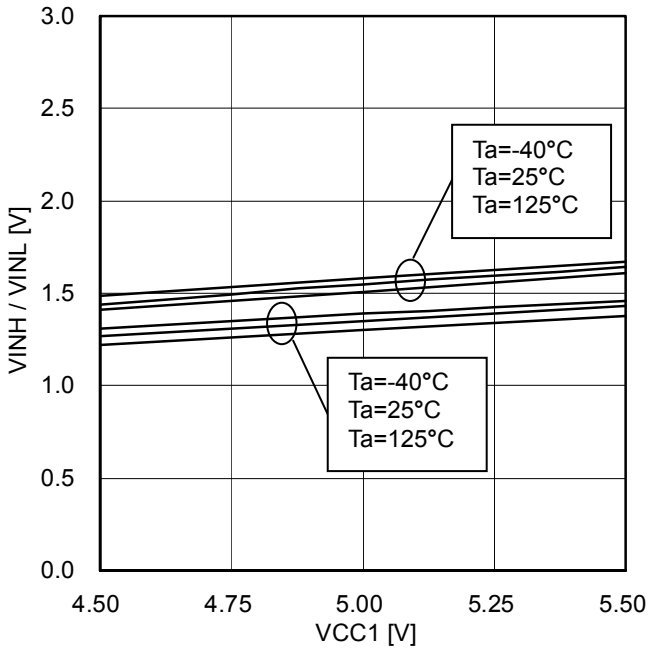


Figure 19. Logic（IN/ENA) High/Low level input voltage

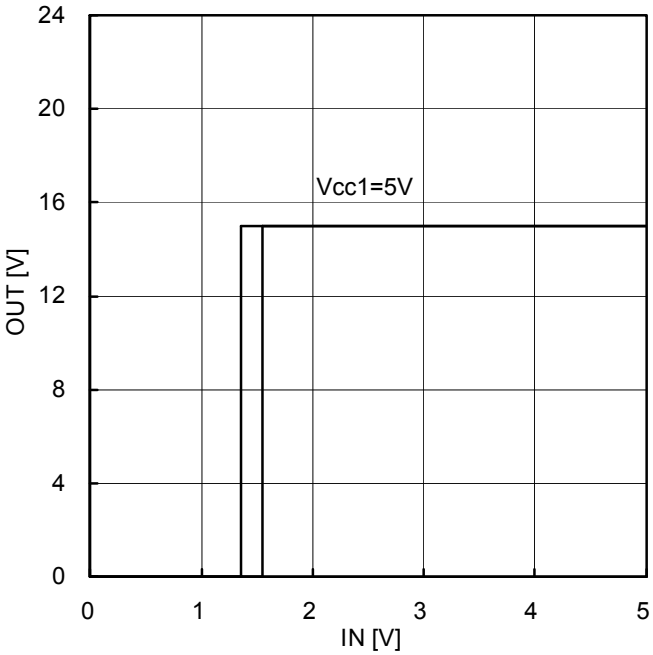


Figure 20. Logic（IN/ENA) High/Low level input voltage at Ta=25°C

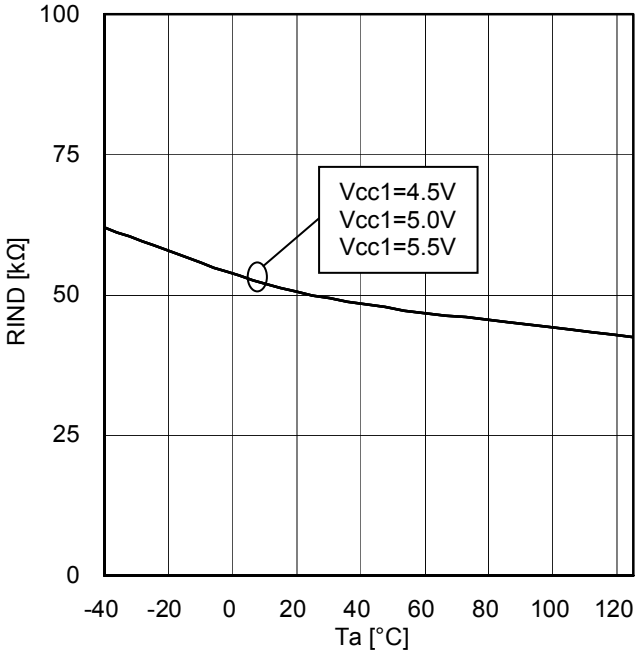


Figure 21. Logic pull-down resistance

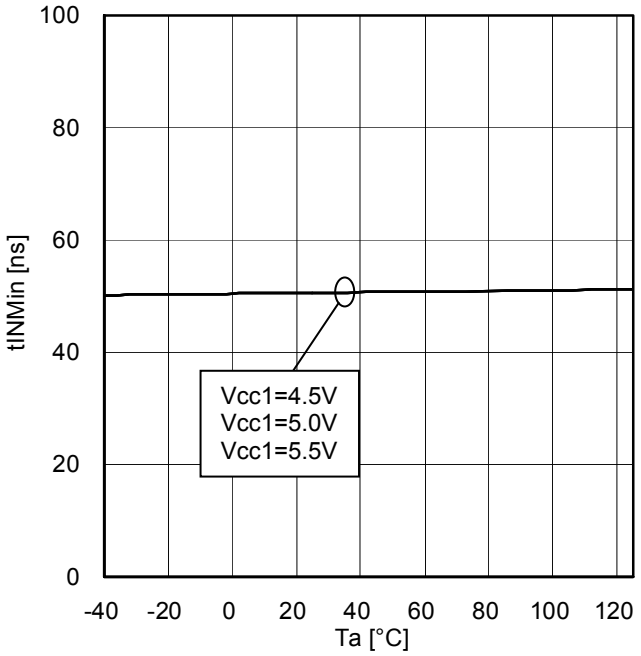


Figure 22. Logic input minimum pulse width

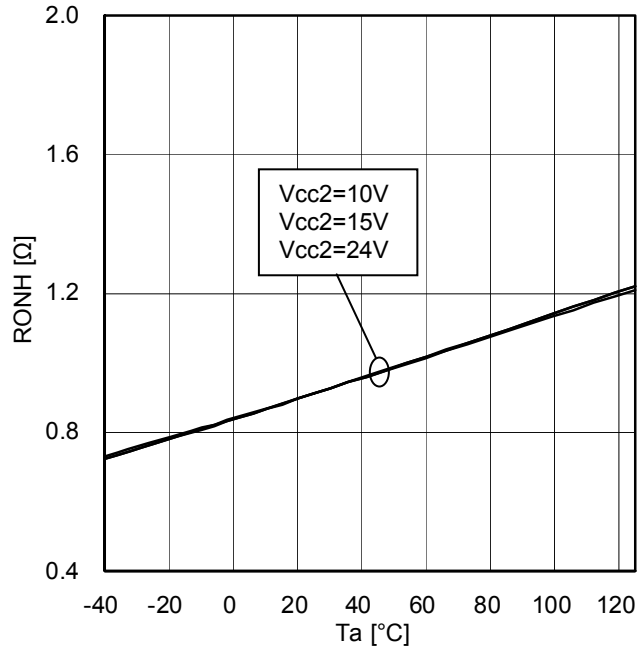


Figure 25. OUT ON resistance (Source)

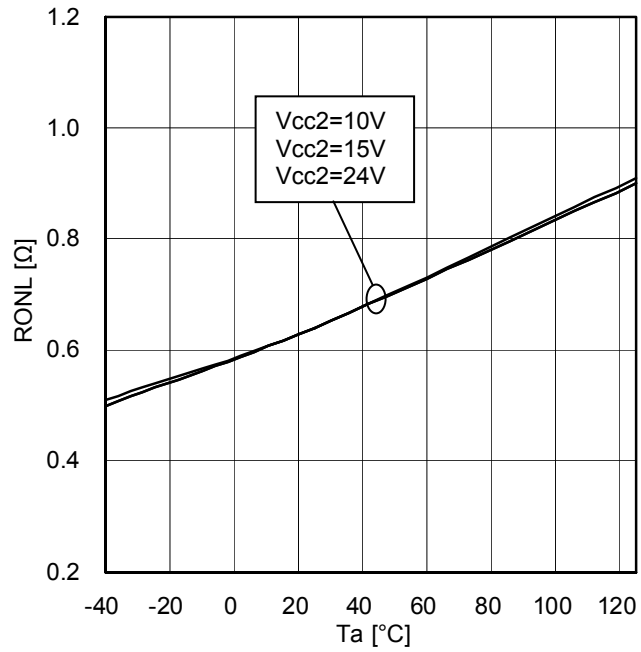


Figure 26. OUT ON resistance (Sink)

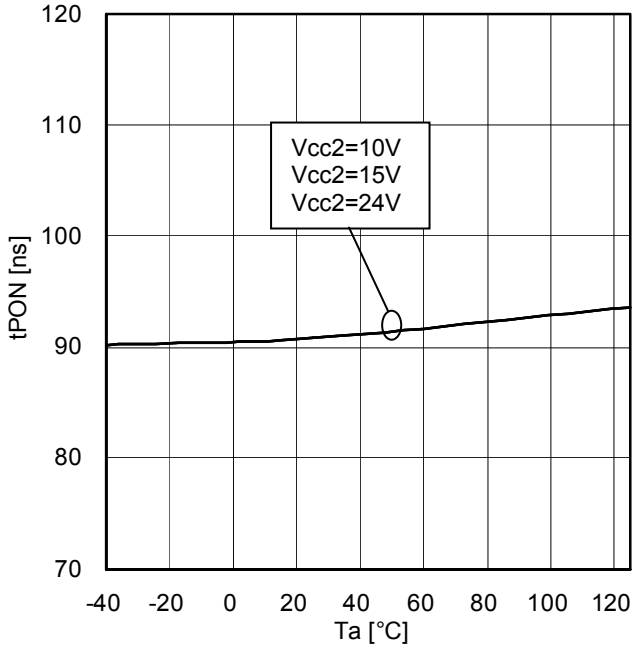


Figure 27. Turn ON time

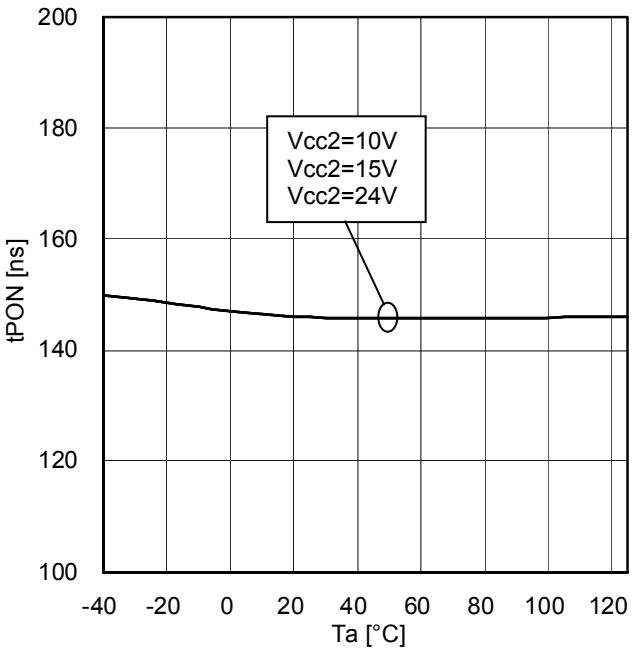


Figure 28. Turn OFF time

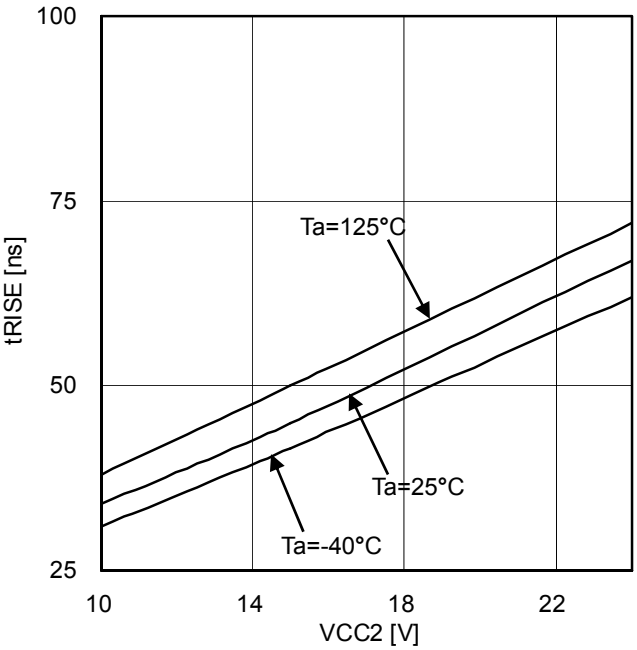


Figure 29. Rise time
（10,000pF between OUT-GND2）

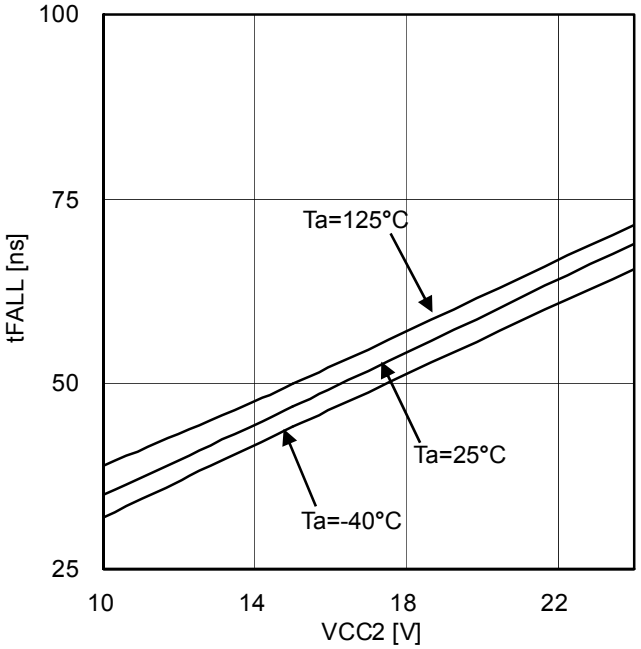


Figure 30. Fall time
（10,000pF between OUT-GND2）

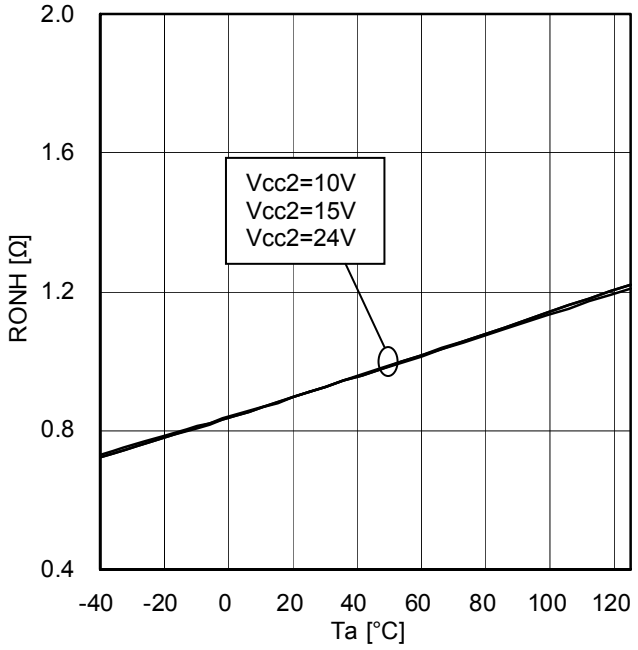


Figure 31. MC ON resistance

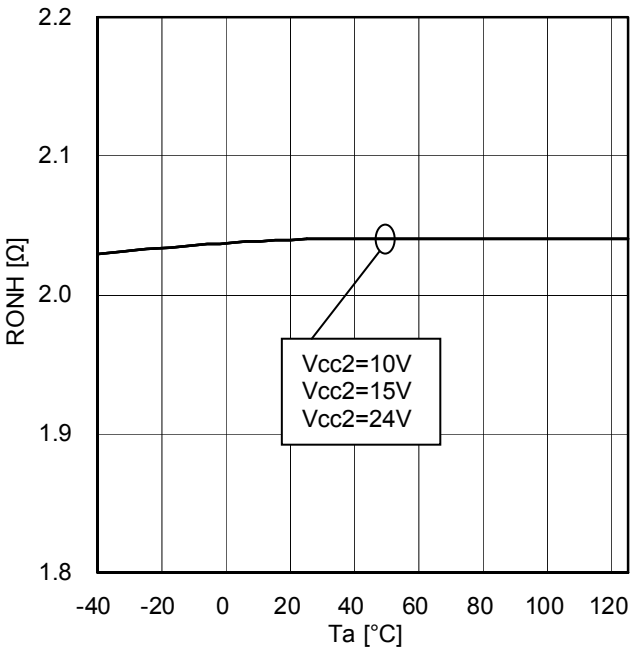


Figure 32. MC ON threshold voltage

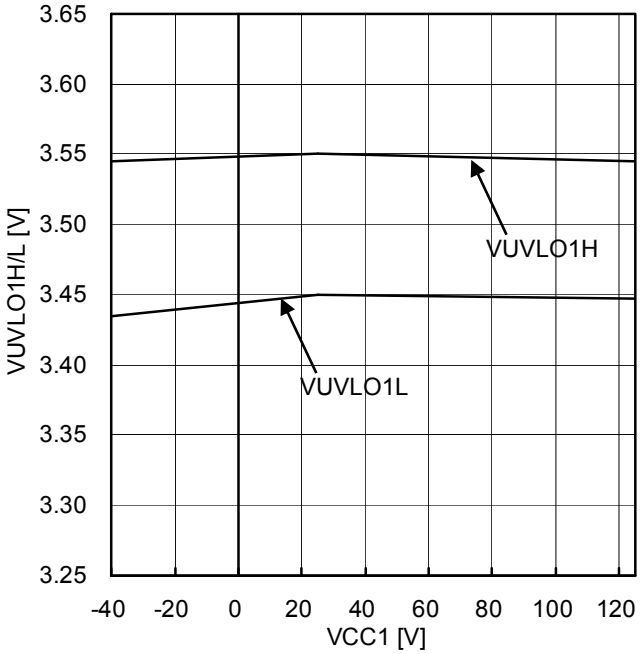


Figure 33. VCC1 UVLO ON/OFF voltage

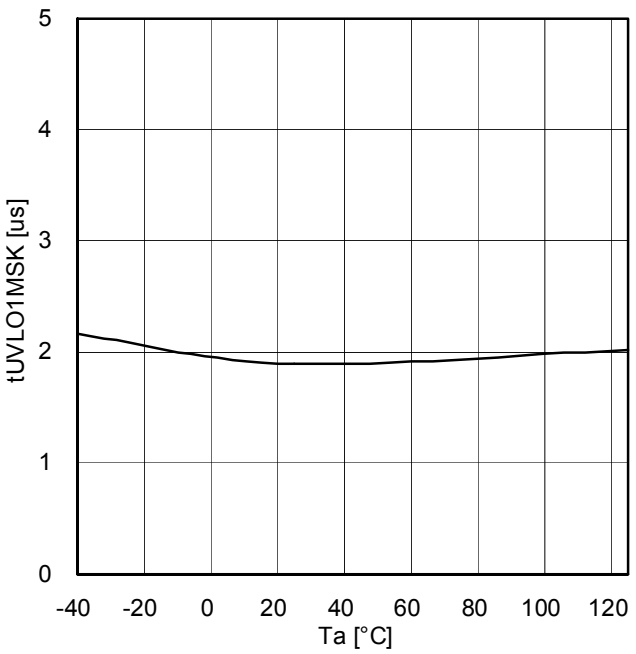


Figure 34. VCC1 UVLO mask time

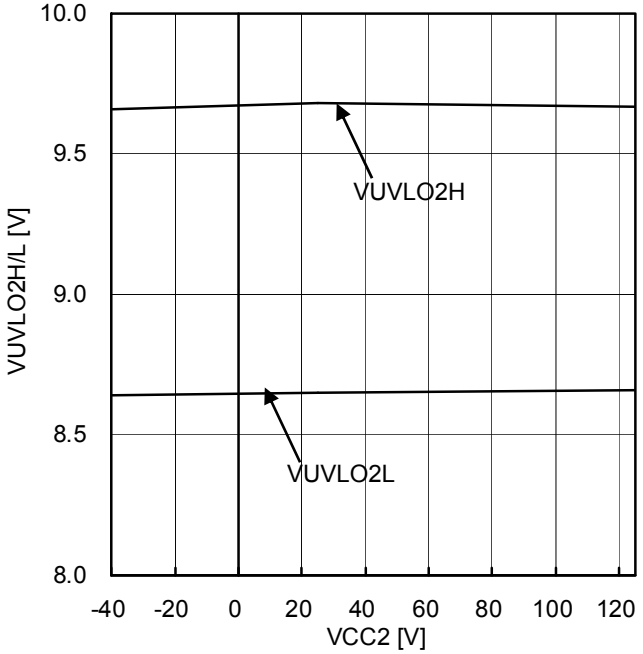


Figure 35. VCC2 UVLO ON/OFF voltage
(at VCC1=5V)

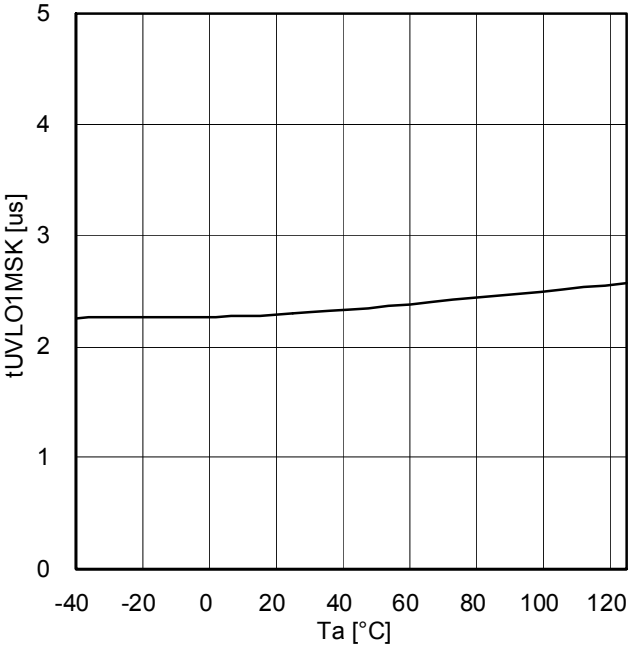


Figure 36. VCC2 UVLO mask time

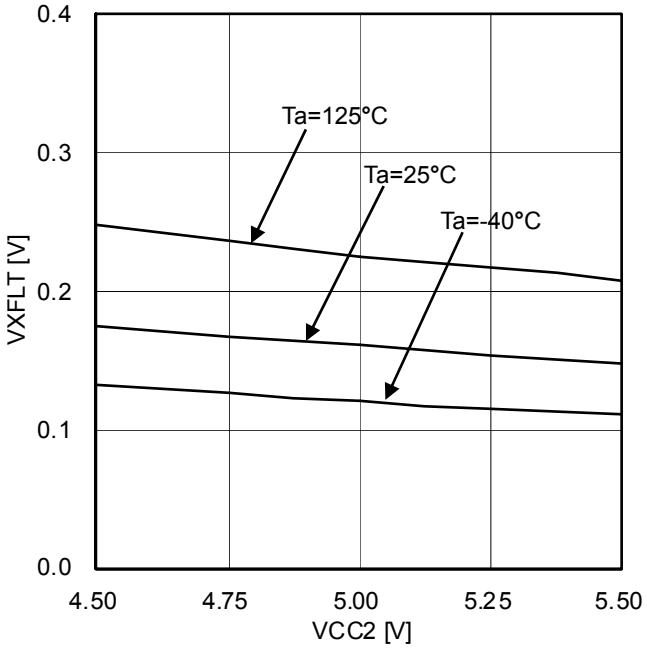
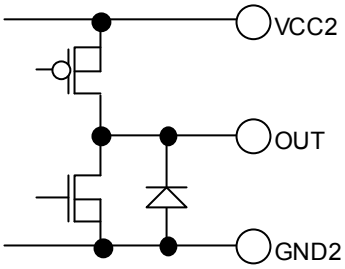
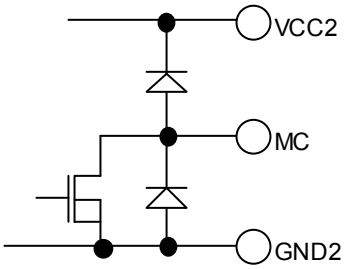
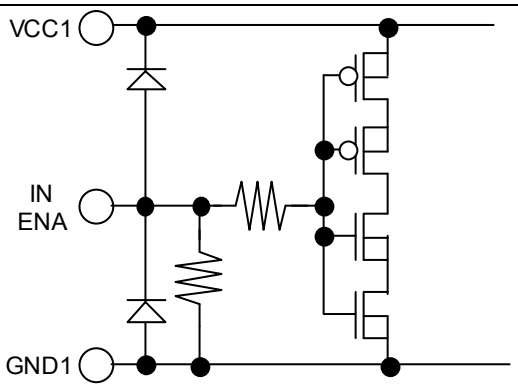
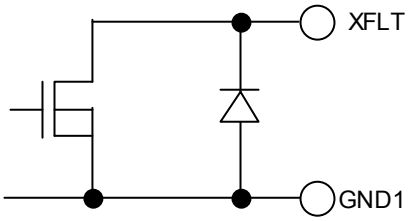


Figure 37. XFLT output Low voltage（IXFLT=5mA）

●I/O equivalence circuits

Pin No	Name / Function	I/O equivalence circuits
1	OUT Output pin	
2	MC Output pin for Miller clamp	
3	IN Control input pin ENA Input enabling signal input pin	
4	XFLT Fault signal output pin	

●**Power Dissipation**

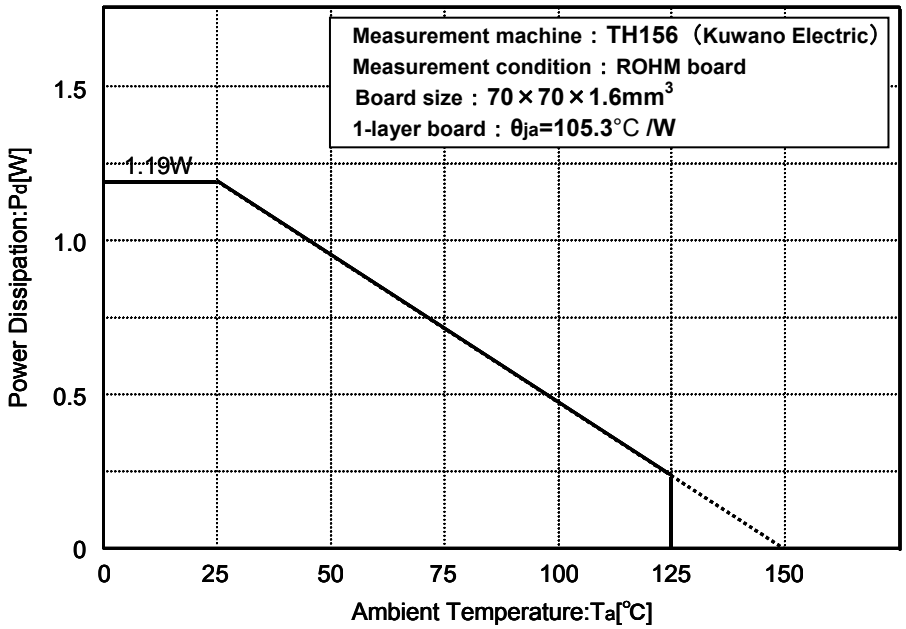


Figure 38. SSOP-B20W Derating Curve

●**Thermal design**

Please confirm that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly obeyed under all circumstances.

●Operational Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND1 Potential

The potential of GND1 pin must be minimum potential in all operating conditions. (Input side ; 11pin to 20pin)

(5) GND2 Potential

The potential of GND2 pin must be minimum potential in all operating conditions. (Output side ; 1pin to 10pin)

(6) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(7) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(8) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(9) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(10) Input terminal of IC

Between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.

For example, when the resistance and transistor are connected to the terminal as shown in figure 10,

- ○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
- ○Also, when GND＞(Terminal B) at the transistor (NPN), The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

(11) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

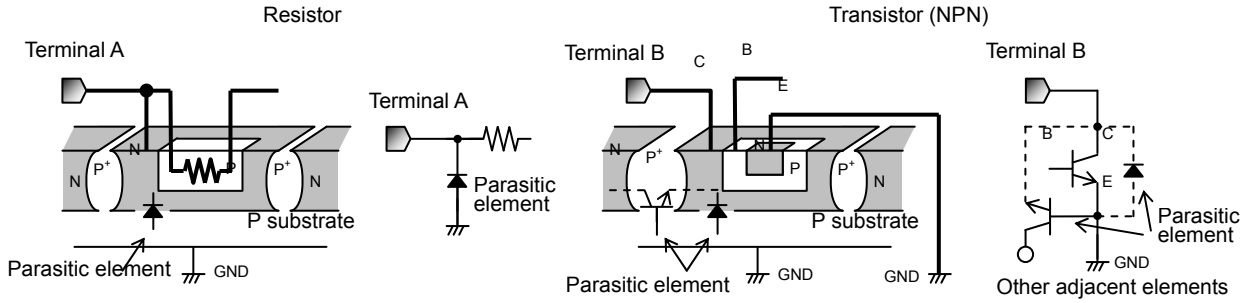


Fig.39 Pattern Diagram of Parasitic Element

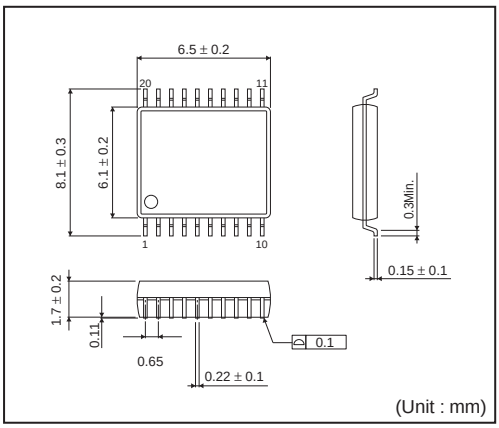
●Ordering Information

B M 6 0 0 1 4 F V	-	CE 2

- Part Number
- Package FV: SSOP-B20W
- Packaging and forming specification E2: Embossed tape and reel

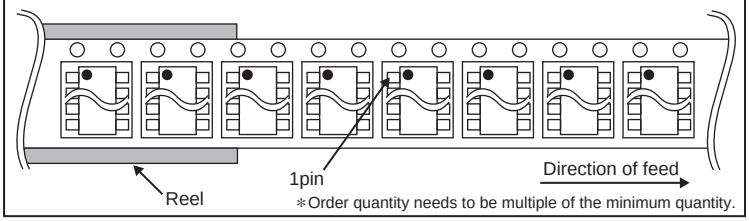
●Physical Dimension Tape and Reel Information

SSOP-B20W



<Tape and Reel information>

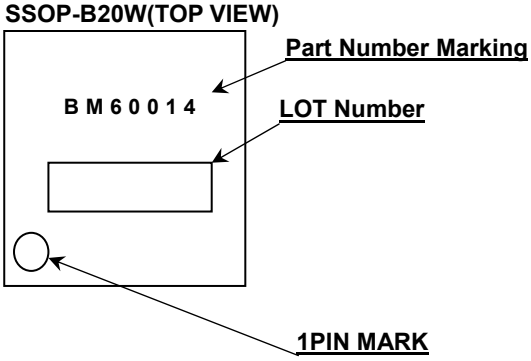
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams (TOP VIEW)

SSOP-B20W(TOP VIEW)



●**Revision History**

Date	Revision	Changes
2012.1.8	001	New Release
2012.1.10	002	P.1 Add the Fault signal output function
		P.1 Change Minimum input pulse width
		P.1 Figure1. Change Application circuits
		P.2 Add the XFLT pin
		P.3 Add Description of the XFLT pin
		P.5 Change UVLO operation timing chart
		P.6 Change I/O condition table
		P.6 Change Power supply startup / shutoff sequence
		P.7 Change Absolute Maximum Ratings
		P.8 Change Minimum input pulse width
		P.8 Change Turn ON/OFF time
		P.8 Add XFLT output L voltage
		P.10 Add Fault signal output pin
2012.1.24	003	P.4 Change Figure3. Block diagram of Miller Clamp function
		P.7 Change Absolute Max Ratings and Recommended Operating Ratings of VCC2
2013.2.7	004	P.3 Change Description of INA and ENA pin
		P.6 Add description of symbol of I/O condition table
		P.8 Change VCC2 rate of Electrical Characteristics
		P.8 Change IN-OUT Timing Chart
		P.10 Change I/O equivalence circuits of IN and ENA
2013.4.11	005	P.1 Change I/O delay time
		P.1 Change Minimum input pulse width
		P.7 Delete MC pin output current (Peak 10 μ s)
		P.8 Delete Input side circuit current(OUT=L)
		P.8 Change the limit of Input side circuit current(OUT=10kHz, 20kHz)
		P.8 Change the limit of Logic input minimum pulse width
		P.8 Change the limit of OUT ON resistance (Sink)
		P.8 Change the limit of Turn ON/OFF time
		P.8 Change the limit of MC ON resistance
		P.8 Delete MC output delay time
		P.8 Change the limit of VCC1 UVLO mask time
		P.8 Change the limit of XFLT output L voltage
2013.5.10	006	P.9 - P.15 Add Typical Performance Curve
2013.6.25	007	P.8 Add the OUT maximum current (Sink)
		P.8 Change the limit of MC ON resistance
		P.8 Change the limit of VCC1 UVLO mask time
		P.8 Change the limit of VCC2 UVLO mask time