Maximum voltage 80V 2ch Gate Driver

BD6566TL

General Description

The BD6566TL is a gate driver with I/O delay time of 55ns, and minimum input pulse width of 50ns, and incorporates undervoltage lockout (UVLO) function.

Features

- 2ch Gate Driver
- Undervoltage lockout function
- Half Bridge/ 2ch Low-side/ 2ch High-side compatible

Applications

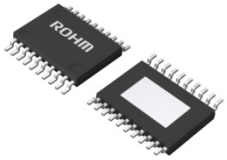
- Half Bridge Gate drive
- 2ch Low-side Gate drive
- 2ch High-side Gate drive

Key Specifications

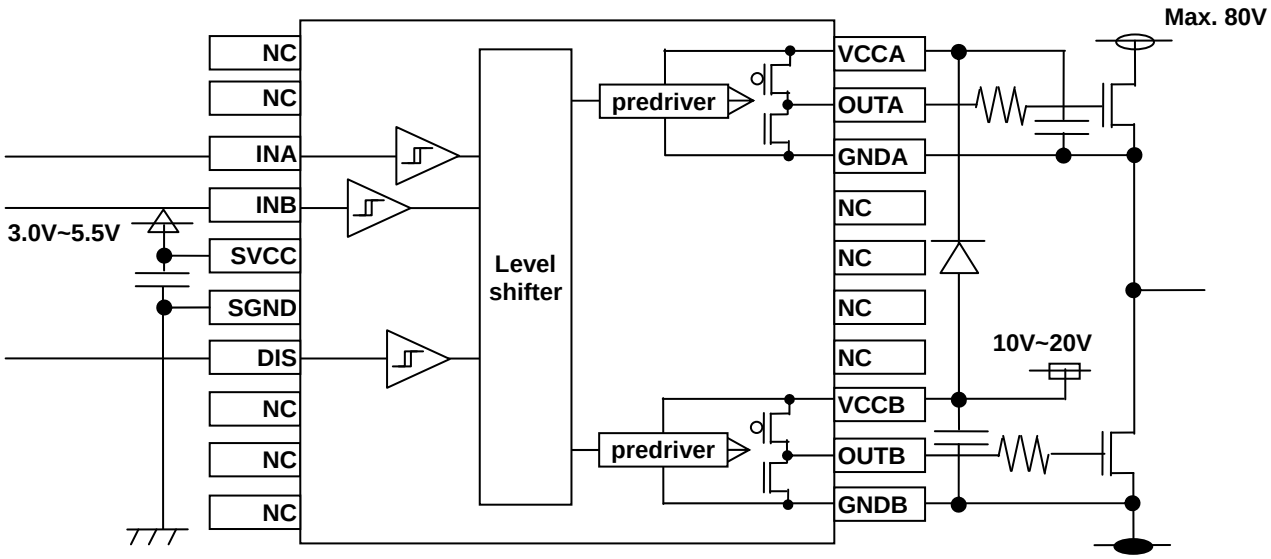
- Maximum GNDA/GNDB voltage: 80V
- Maximum gate drive voltage: 20V
- I/O delay time: 55ns(Max.)
- Minimum input pulse width: 50ns(Max.)

Package

	W(Typ.) x D(Typ.) x H(Max.)
HTSSOP-B20	6.50mm x 6.40mm x 1.00mm



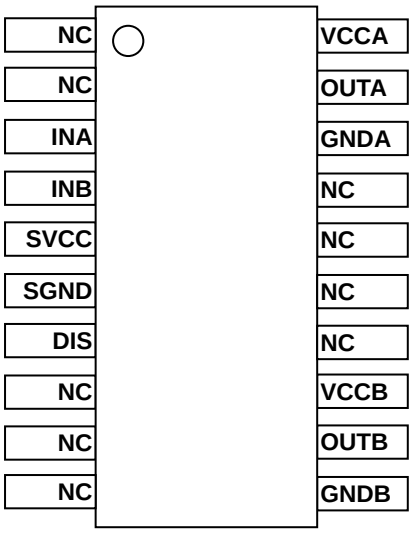
Typical Application Circuit



Recommended range of external constants

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
SVCC	C_{SVCC}	0.01	-	-	uF
VCCA	C_{VCCA}	0.01	-	-	uF
VCCB	C_{VCCB}	0.01	-	-	

Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	NC	NC
2	NC	NC
3	INA	Ach Control signal input pin
4	INB	Bch Control signal input pin
5	SVCC	Power supply pin for signal input
6	SGND	Ground pin for signal input
7	DIS	Input disabling signal input pin
8	NC	NC
9	NC	NC
10	NC	NC
11	GNDB	Ground pin for Bch gate drive
12	OUTB	Output pin for Bch gate drive
13	VCCB	Power supply pin for Bch gate drive
14	NC	NC
15	NC	NC
16	NC	NC
17	NC	NC
18	GNDA	Ground pin for Ach gate drive
19	OUTA	Output pin for Ach gate drive
20	VCCA	Power supply pin for Ach gate drive

Description of pins and cautions on layout of board

1) SVCC (Power supply pin for signal input)
The SVCC pin is a power supply pin for signal input. To suppress voltage fluctuations, connect a bypass capacitor between the SVCC and the SGND pins.

2) SGND (Ground pin for signal input)
The SGND pin is a ground pin for signal input.

3) VCCA and VCCB (Power supply pins for Ach and Bch gate drive respectively)
The VCCA and the VCCB pins are power supply pins for Ach and Bch gate drive respectively. To reduce voltage fluctuations due to OUTA/OUTB pins output current, connect a bypass capacitor between the VCCA/VCCB and the GNDA/GNDB pins respectively.

4) GNDA and GNDB (Ground pins for Ach and Bch gate drive respectively)
The GNDA and GNDB pins are ground pins for Ach and Bch gate drive. Connect the GNDA/GNDB pins to the emitter (or source) of power devices respectively.

5) INA, INB, and DIS (Control input terminal)
The INA, INB and DIS pins are pins used to determine output logic.

DIS	INA	INB	OUTA	OUTB
H	X	X	L	L
L	L	L	L	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	L

6) OUTA and OUTB (Output pin for Ach and Bch gate drive respectively)
The OUTA and OUTB pins are pins used to drive the gate of a power device.

Description of functions and examples of constant setting

1) Undervoltage Lockout (UVLO) function
The BD6564F-C incorporates the undervoltage lockout (UVLO) function both on the input and the output voltage sides. When the power supply voltage for signal input (SVCC) drops to the UVLO ON voltage, the OUTA and OUTB pins both will output the “L” signal. When SVCC rises to the UVLO OFF voltage, these pins will be reset. When the power supply voltage for gate drive (VCCA/VCCB) drop to the UVLO ON voltage, the OUTA and OUTB pins respectively will output the “L” signal. When VCCA/VCCB rises to the UVLO OFF voltage, OUTA and OUTB pins will be reset respectively. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on every power supply pin.

2）I/O condition table

No.	Status	Input						Output	
		SVCC	VCCA	VCCB	DIS	INA	INB	OUTA	OUTB
1	SVCC UVLO	UVLO	X	X	X	X	X	L	L
2	Disable	○	X	X	H	X	X	L	L
3	VCCA and VCCB UVLO	○	UVLO	UVLO	L	X	X	L	L
5	VCCA UVLO	○	UVLO	○	L	X	L	L	L
6		○	UVLO	○	L	X	H	L	H
7	VCCB UVLO	○	○	UVLO	L	L	X	L	L
8		○	○	UVLO	L	H	X	H	L
9	Normal operation	○	○	○	L	L	L	L	L
10		○	○	○	L	H	L	H	L
11		○	○	○	L	L	H	L	H
12		○	○	○	L	H	H	L	L

○: SVCC, VCCA or VCCB > UVLO, X:Don't care

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CCS}	-0.3～+7.0 (Note1)	V
Output-side supply voltage relative to GNDA/GNDB	V_{CCA} /V_{CCB}	-0.3～+24.0 (Note2)	V
Output-side supply voltage relative to SGND	V_{CCA-S} /V_{CCB-S}	-0.3～+90.0 (Note1)	V
Output-side ground voltage	V_{GNDA}/V_{GNDB}	-0.3～+80.0 (Note1)	V
INA, INB, DIS pin input voltage	V_{IN}	-0.3～+SVCC+0.3 or 7.0 (Note1)	V
OUTA/OUTB pin output current (Peak 10us)	$I_{OUTAPEAK}$ /$I_{OUTAPEAK}$	5.0 (Note3)	A
Power dissipation	P_d	3.20 (Note4)	W
Operating temperature range	T_{opr}	-40～+125	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	+150	℃

(Note 1) Relative to SGND.
(Note 2) Relative to GNDA/GNDB.
(Note 3) Should not exceed Pd and Tj=150°C.
(Note 4) Derate above Ta=25°C at a rate of 25.6mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CCS} *5	3.0	5.5	V
Output-side supply voltage	V_{CCA} /V_{CCB} *6	10	20	V

*5 Relative to SGND.
*6 Relative to GNDA/GNDB.

Electrical Characteristics

（Unless otherwise specified Ta=-40℃~125℃, V_{CCS}=3.0V~5.5V, V_{CCA}=V_{CCB}=10V~20V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current	I_{CCS}	30	100	150	uA	
Output side circuit current	I_{CCA}/I_{CCB}	0.2	0.7	1.5	mA	
Logic block						
Logic high level input voltage	V_{INH}	V_{CCS}*0.7	-	V_{CCS}	V	INA, INB, DIS
Logic low level input voltage	V_{INL}	0	-	V_{CCS}*0.3	V	INA, INB, DIS
Login input current	I_{IN}	-1.0	0.0	1.0	μA	INA, INB, DIS
Output						
OUTA/OUTB ON resistance (Source)	R_{ONH}	0.3	0.7	1.5	Ω	I_{OUT}=40mA
OUTA/OUTB ON resistance (Sink)	R_{ONL}	0.2	0.5	1.2	Ω	I_{OUT}=40mA
OUTA/OUTB maximum current	I_{OUTMAX}	3.0	4.5	-	A	Guaranteed by design
Turn ON time	t_{PON}	30	45	60	ns	
Turn OFF time	t_{POFF}	30	45	60	ns	
Propagation distortion	t_{PDIST}	-10	0	10	ns	t_{POFF} - t_{PON}
Rise time	t_{RISE}	6	12	18	ns	2nF Load, Guaranteed by design
Fall time	t_{FALL}	6	12	18	ns	2nF Load, Guaranteed by design
Channel-to-Channel matching	t_{PAB}	-10	0	10	ns	
Protection functions						
SVCC UVLO OFF voltage	V_{UVLO1H}	-	-	3.0	V	
SVCC UVLO mask time	$t_{UVLO1MSK}$	0.4	1.0	3.0	μs	
VCCA/VCCB UVLO OFF voltage	V_{UVLOAH} /V_{UVLOBH}	7.5	8.5	9.4	V	
VCCA/VCCB UVLO ON voltage	V_{UVLOAL} /V_{UVLOBL}	7.0	7.8	8.5	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	0.4	1.0	3.0	μs	

Typical Performance Curves

TBD

Power Dissipation

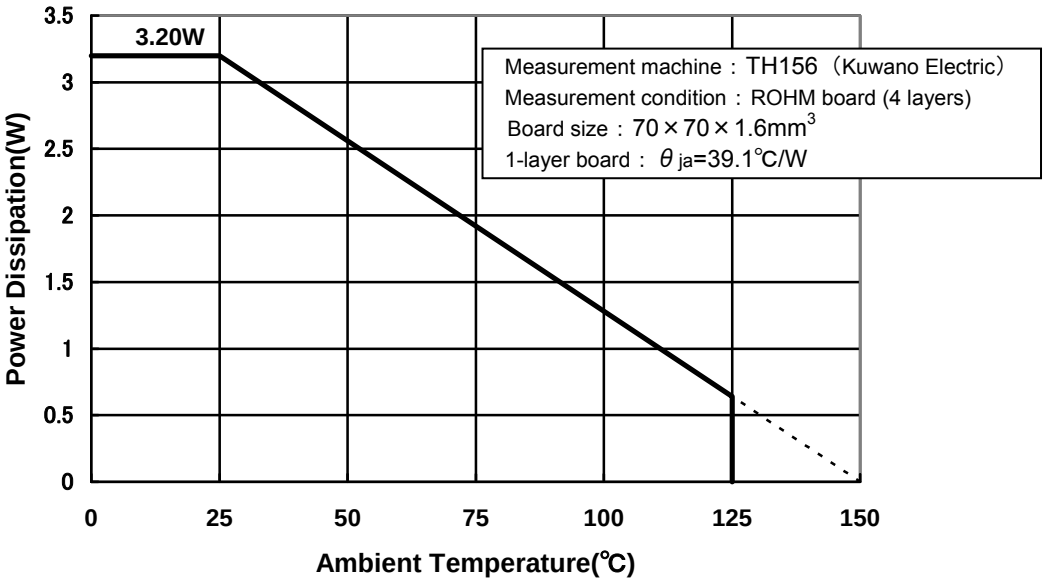
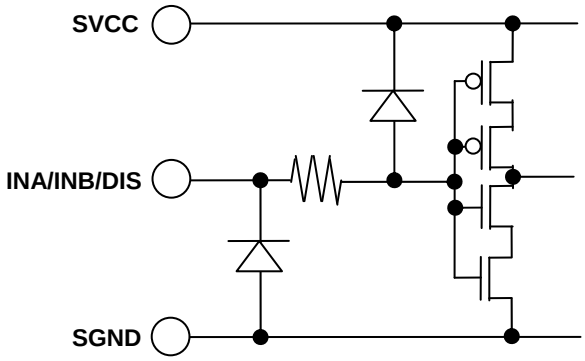
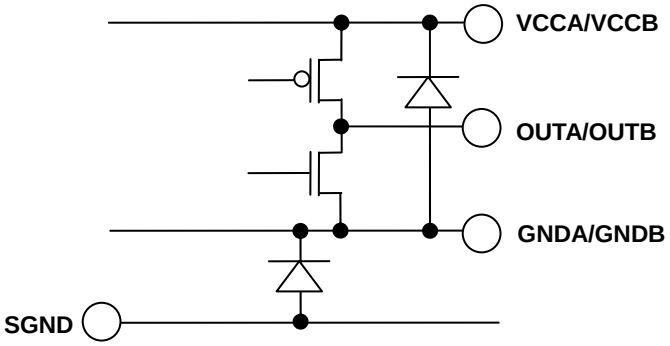


Fig.xx HTSSOP-B20 Derating Curve

Thermal design

Please confirm that the IC's chip temperature Tj is not over 150℃, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150℃ is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150℃ must be strictly obeyed under all circumstances.

I/O equivalence circuits

Pin No.	Name / Function	I/O equivalence circuits
3	INA Ach Control signal input pin	
4	INB Bch Control signal input pin	
7	DIS Input disabling signal input pin	
12	OUTB Output pin for Bch gate drive	
19	OUTA Output pin for Ach gate drive	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent from exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

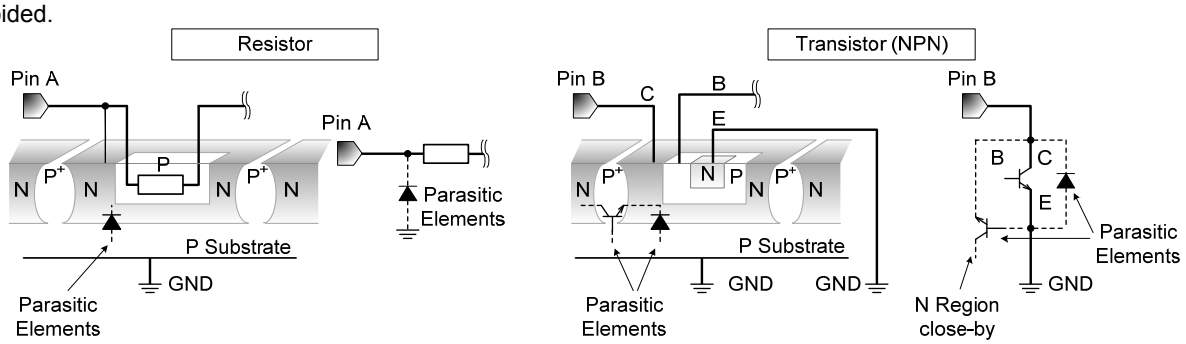


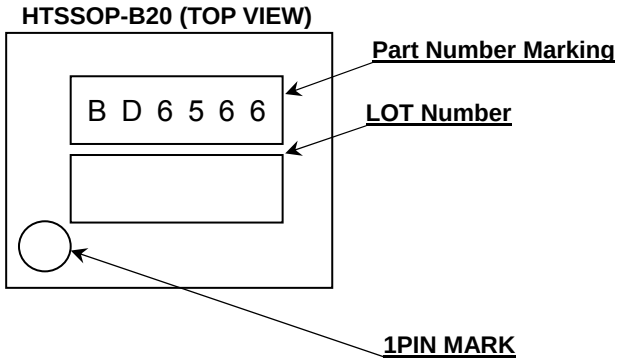
Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

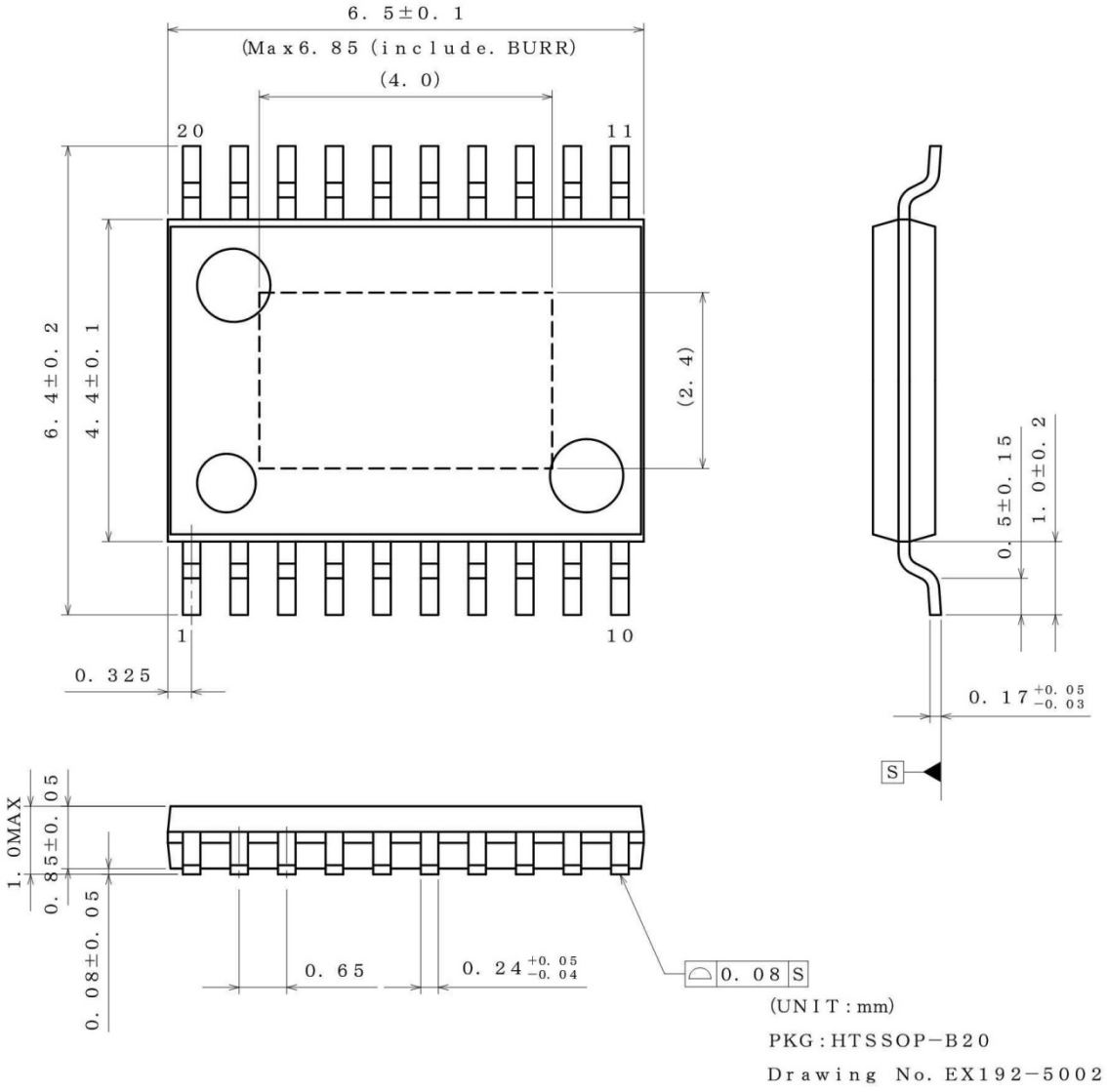
Ordering Information

Marking Diagrams



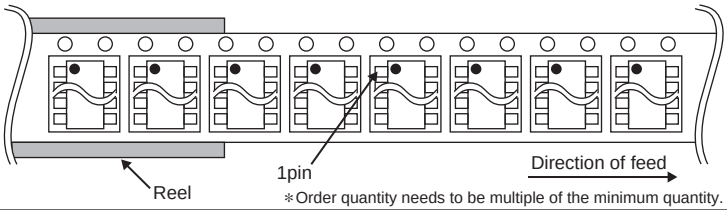
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
31.Jul.2013	001	New Release