Description and Application Manual for PHD515-17 high power IGBT gate driver

WEPOWER series high power IGBT intelligent driving modules are specially designed for high power IGBT module with high reliability and security. The products series have been patented in China.

The high power IGBT intelligent module driver released by WEPOWER is easy to use with smart design, high driving power and complete function. The simplest drive method is allowed by PHD515-17 to drive max power tube IGBT and parallel circuit. With high voltage isolation, it also can drive high voltage IGBTs module and series IGBTs. Through fiber optic cable transmit signals with very short time, PHD515-17 can be used for high voltage frequency inverters and high frequency power supply and RF converter and resonance converter. PHD515-17 HV high power IGBT intelligent drive module can drive high power IGBTs of 1700V. It is Pin-to-Pin compatible with CONCEPT IGD515.

Applications

※ Traction
※ Power Converters
※ Motor Drives
※ Switch Mode Power Supplies
※ Radiology and Laser Technology
※ High Frequency Applications
※ Wind Power Converter
※ High Voltage Converters
※ RF Generators and Converters
※ Railway Power Supply
※ Induction Heating

1. Main Features & Technical Specifications

1.1 Main Features

(1) Suitable for driving high voltage IGBT module
(2) Short circuit and over current and under-voltage protection.
(3) Reliable and durable
(4) High electrical isolation
(5) Switching frequency: 0~100KHz
(6) Duty ratio: 0~100%
(7) Disturbance rejection property: dv/dt >100,000V/us
(8) Integrated internal DC/DC power supply

1.2 Technical Specifications

IGBT Block Voltage：≤1700V；
Rated Input Voltage：15V（±0.5V）；
Max Driving Current：±16A；
Internal DC/DC Power：5W；
Rated Driving Voltage：+15V/-15V；
Operation Temperature Range：
PHD515-17I：-40℃～+85℃
PHD515-17J：-40℃～+105℃
PHD515-17M：-55℃～+125℃

Max Rating			
Symbol	Definition	Value	Unit
VDC	voltage supply primary input side	15.6	V
V_{iH}	Input signal voltage (high)	5+0.5	V
V_{iL}	Input signal voltage (low)	GND-0.3	V
$Iout_{PEAK}$	Output gate peak current	16	A
$Iout_{AVmax}$	Output average current	350	mA
f_{max}	Max switch frequency	100	kHz
V_{CE}	Collector emitter voltage sense across the IGBT	1700	V
dv/dt	Rate of rise and fall of voltage secondary to signal primary side	50	kV/us
V_{isolIO}	Isolation test voltage input-output (AC,RMS,10S)	8	kV
R_{Gonmin}	Minimum rating for R_{Gon}	1	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	1	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse	60	uC

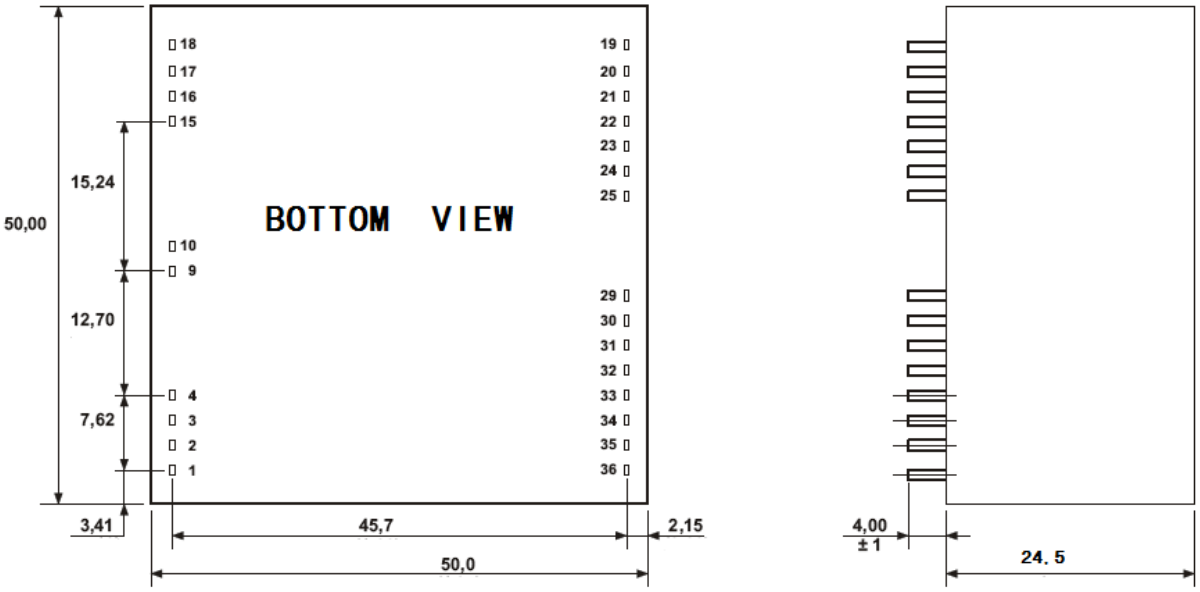
T_{op}	Operation Temperature	PHD515-17I	-40℃～+85℃	℃
		PHD515-17J	-40℃～+105℃	
		PHD515-17M	-55℃～+125℃	
T_{stg}	Storage Temperature	PHD515-17I	-55℃～+105℃	℃
		PHD515-17J	-55℃～+125℃	
		PHD515-17M	-60℃～+130℃	

Electrical characteristics

Symbol	Definition	Value			Unit
		Min.	Typ.	Max.	
VDC	voltage supply DC/DC converter	14.5	15	15.6	
I_{SO}	Supply current primary side (no load)		80		mA
	Supply current primary side (max)			450	mA
$V_{G(on)}$	Turn on gate voltage output		+15		V
$V_{G(off)}$	Turn off gate voltage output		-15		V
I_{OMAX}	Max drive current		16		A
$t_{d(on)}$	Turn-on propagation time		110		ns
$t_{d(off)}$	Turn-off propagation time		100		ns
$t_{r(out)}$	Output rise time		40		ns
$t_{f(out)}$	Output fall time		40		ns
$t_{d(err)}$	Error propagation time			300	ns
C_{PS}	Coupling capacitance primary secondary		10		pF
W	Weight		48		g
MTBF	Mean time between failure (Ta=40℃,max load)		2.0		10^6h

2. PHD515-17 Block Diagram

TOP VIEW

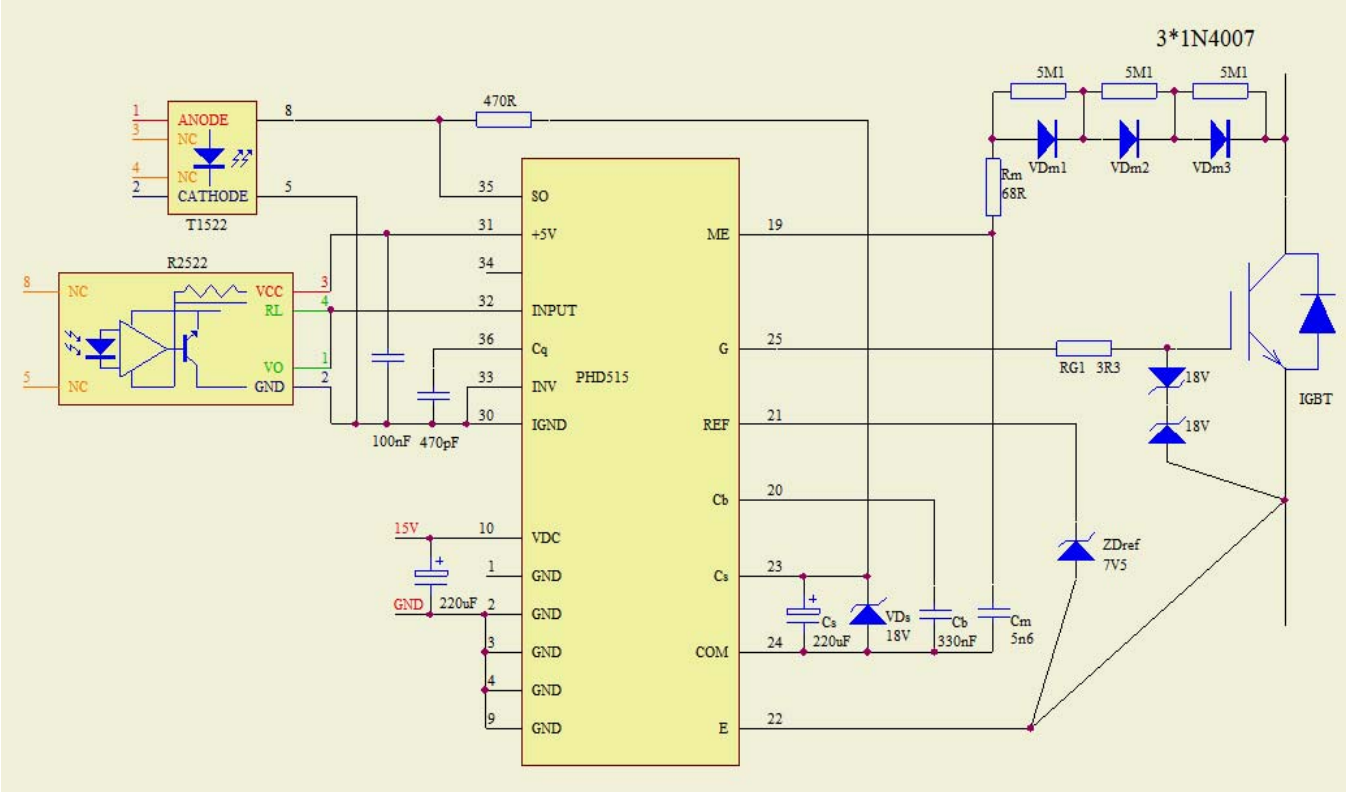


PHD515-17 Dimensional Diagram

Pin	Function	Pin	Function
1 GND	Low voltage terminal power	12 NC	
2 GND	Low voltage terminal power	13 NC	
3 GND	Low voltage terminal power	14 NC	
4 GND	Low voltage terminal power	15 NC	
5 NC		16 NC	
6 NC		17 NC	
7 NC		18 NC	
8 NC		36 Cq	Acknowledgement pulse Capacitor
9 GND	Low voltage terminal power	35 SO	Error Output
10 VDC 15V	Low voltage terminal power	34 SDOSA	Series Connection Mode selection
11 NC			

33 INV Input Negated	25 G G collector output
32 INPUT Signal input	24 COM Common
31 +5V 5V output	23 CS 15V
30 IGND Signal terminal	22 E E collector
29 NC	21 REF Over current threshold setting
28 NC	20 Cb Blocking time setting capacitor
27 NC	19 ME V_{CE} Detection
26 NC	

3. Application example



PHD515-33 Typical Application Circuit

4. Overview of WEPOWER High Power IGBT Intelligent Driving Module

(1) More reliable operation (Gate bipolar power supply with +15V/-15V is suitable for IGBT of any manufacturer. The gate is driven by negative voltage which increases capacity of anti-interference and more Parallel IGBTs can be driven.)

(2) True electrical isolation. (The transformer isolation technology is used for each channel of drivers to reach better insulation properties and lower coupling capacitance.)

5. Operation Principle

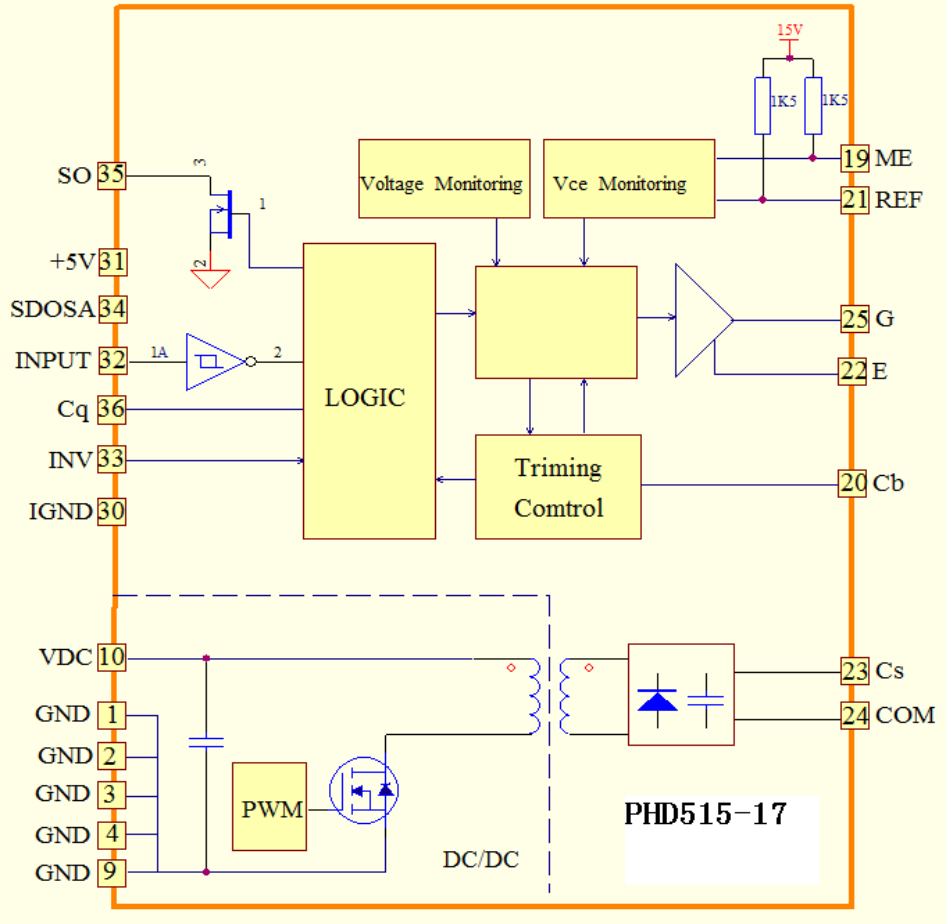
5.1 Block diagram

PHD515-17 high-power IGBT intelligent driving module mainly consists of internal DC / DC converting circuit and IGBT Intelligent driving circuit which is formed by a logic processing circuit, a power drive and detection circuits.

Integrated DC / DC power supply

All of the standard series of WEPOWER high-power IGBT intelligent drive module includes a DC / DC converter for each channel to provide drive voltage. Therefore, drivers need only a stable 15V DC power supply. As for different application, especially the different switching frequency and power valve gate charge, WEPOWER offers different driving power. Internal DC/DC drive power of PHD515-17 is 5W.

The block diagram is shown below:



5.2 Protection Features

The IGBT V_{CE} detection circuit is set in PHD515-17 high power intelligent driver. Once the V_{CE} value exceeds setting voltage of gate or fault of under-voltage is detected, shutdown signal will generated by the module immediately. The drive board begins to turn off the power tube and no longer receive any driving signal. SO output is low level. The driver will not accept any driving signal until the "blocking" time has elapsed and then to restart. Error blocking time can be set by Cb.

5.3 Operation Mode

PHD515-17 high-power driver provides selection for series connection working mode. Pin SDOSA is the selection terminal for series connection and in normal condition it is vacant. When over-current happens for IGBTs, the driver will turn off immediately and transmits the status to SO. When +5V is connected to SDOSA, IGBTs are in-series mode. When over-current happens for IGBTs, IGBTs are not turned off, it only transmits status to SO and pass to control part of the system by optical fiber, then the system will shut off all the IGBTs.

5.4 The Pin Designation

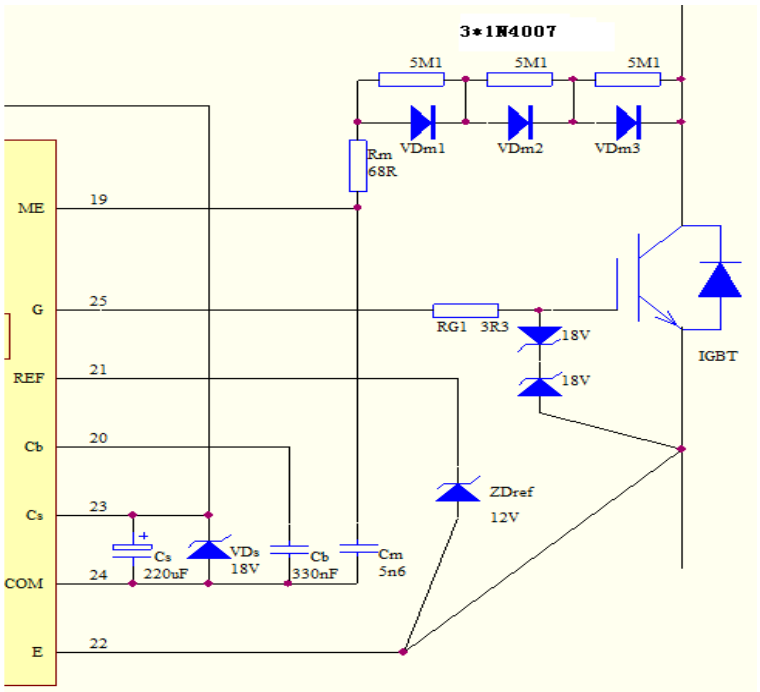
5.4.1 The Input Side

Pin GND
Pin GND is connected to the ground of the electronic power supply.

Pin VDC (+15V voltage supply of input side)
Filtering capacitor 220uF/25V is suggested to be connected between VDC and ground.

5.4.2 The Power Side

Pin ME
This Pin is used to measure the voltage drop at the turned-on power transistor in order to ensure protection against short circuit and overload. It should be noted that it must never be connected directly to the drain or collector of the power transistor. To protect the measurement terminal from the high drain or collector voltage of the turned-off power element, a circuit with high-blocking diodes (Dme) or several diodes connect in series should be included. It is absolutely recommended to over dimension these diodes in terms of voltage.



A pull-up resistor intergrated in the driver module ensures that a current flows through the measurement diode (Dme), the resistor (Rme) and the power transistor when the latter is turned on. A potential is then present at the measurement input ME that corresponds to the forward voltage of the turned-on transistor plus the diode forward voltage and the voltage drop at Rme. Rme attenuates the reverse-current peaks of the measurement diode Dme and should have a value of about 68Ω.

It should be noted that the power transistor do not turn on immediately. It can take several microseconds for them to switch through fully, especially with IGBTs. Together with the integrated pull-up resistor and the external capacitor (Cme), this produces a delay in the measurement after the power transistor has switched on. This delay shall henceforth be known as the response time. This response time (and thus Cme) must be selected to be greater in inverse proportion to the speed at which the power transistor turn on.

The calculation formula for this responsible as below:

$$C_{me} = \frac{t_a}{1{,}5k\Omega \ \ln\left(\frac{V_{cc}}{V_{cc} - V_{ref}}\right)}$$

Pin Cb

After the current monitoring circuit responds, an error message is reported via the status output SO during a defined time –known henceforth as the blocking time. In normal mode the power transistor is also turned off by the intelligent driver's protection function and remains in this state during the blocking time. This function is used to protect the component from thermal overload at a continuous or repeated short circuit. The blocking time can be determined by connecting Pin 20 (Cb) to Pin 24 (COM) via a capacitor. The calculation formula for Cb as below:

$$C_b = \frac{t_b}{100k\Omega \quad \ln\left(\frac{2 \cdot V_{cc}}{V_{ref}}\right)}$$

Pin REF

An external zener diode is connected to this pin as a reference. This defines the maximum voltage drop at the turned-on power transistor at which the protective function of the driver circuit is activated.

The protection function of the intelligent drivers PHD515-33 series always become active when the voltage at ME (measurement drain / collector) is higher than that at REF.

The reference potential is the emitter (or source) of the power transistor. The reference must never under any circumstances be capacitively blocked. The reference diode should be placed as closed as possible to the driver module.

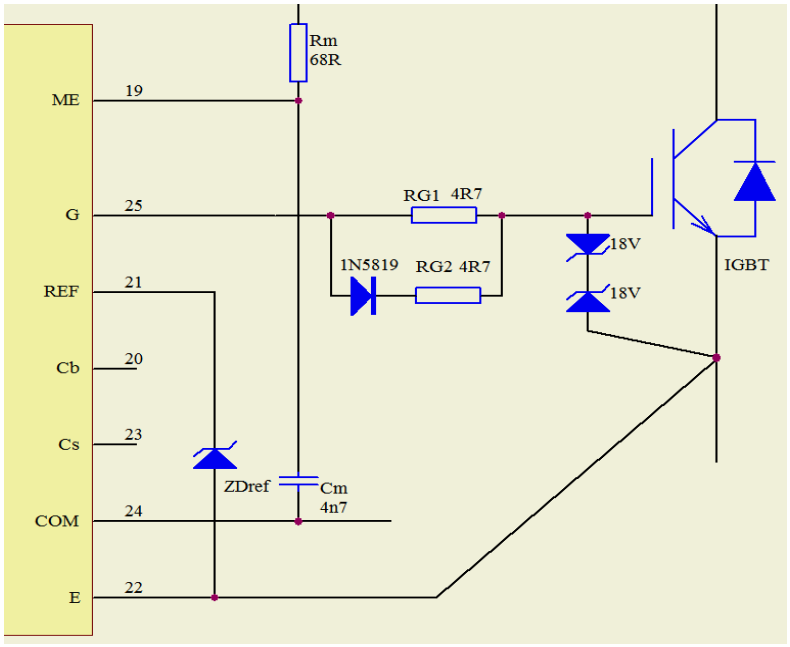
Pin E: E collector output terminal

Pin Cs: 15V output terminal

It can supply power to error feedback optical fiber. A filter capacitor 220uF/25V is recommended to connect Cs and COM.

Pin G: G collector output terminal

Try to use shorter lead wire as possible to connect G collector from IGBTs to Pin 25. Two gate electrode resistors and a diode compose a gate electrode circuit which used to ensure the switch speed for turn on and turn off respectively.



Anisomerous gate pole resistor

Reverse connection a zener diode (18V) between collector G and E in order to avoid engendering stray voltage and over rated gate pole voltage to break IGBTs. Pin G connected to G & E of IGBTs. Connection lead wire can be as shorter as possible and it would be best to be connected with Pin 22 directly with driver module. It is better to use twisted wire to connect G, E and C of IGBTs.

Pin IGND
This Pin is the ground Pin for the interface electronics, especially for the FOL receiver.

Pin +5V: Terminal +5V
A voltage of +5V with respect to IGND is applied to this Pin.
Filtering capacitor 100uF is suggested to be connected between +5V and IGND.

Pin INPUT
It is recommended to receive signal by FOL.

Pin INV
This Pin allows the input signal INPUT to be Negated.
Through this Pin to control INPUT signal reversal. When connect to low level, Pin INPUT with low level effective. When connect to high level, Pin INPUT with high level effective.

Pin SDOSA (Series connection mode selection)

This Pin is used for mode selection and affects the reaction of the protection function.

In normal operation, the SDOSA terminal remains open. This has the effect that when a fault occurs, the power semiconductor is immediately turned off, even if the input signal continues to be applied. The fault status is simultaneously reported to the control electronics via the status output SO.

The second operating mode is designed especially for the series connection of power IGBTs and MOSFETs. For this mode, the SDOSA input is connected to +5V. This has the effect that when an error occurs, the power semiconductor is not turned off. The status output SO merely reports the error status to the control electronics, which must now centrally turn off all the drivers simultaneously quickly as possible or in a given sequence. This is the only way of ensuring the symmetry in the series circuit even if a protective function is triggered.

This function can also be used in bridge circuits, for example to ensure that all power semiconductors are turned off simultaneously in the case of a fault.

Pin SO

This Pin is the status output of the driver. A FOL transmitter for the status acknowledgement is connected to it via a resistor. The supply voltage should be obtained from Pin 23 (Cs). A voltage of about +15V present here. The status output SO has the following status:

If the supply voltage is too low, then the FET at output SO is through connected. This means that no current flows through the FOL transmitter.
If the supply voltage but no error status is applied, then the output SO has high impedance. This means that a current flows through the FOL transmitter of the status acknowledgement circuit.

After the protection function of the driver has detected an error status, the output SO is through connected for the duration of the blocking time. The error status is thus reported to the control electronics.

This output also acknowledges every switching edge of the driving signal with a short pulse, during which the FET becomes conducting. The length of the acknowledgement pulse is determined by connecting Pin Cq to a capacitor.

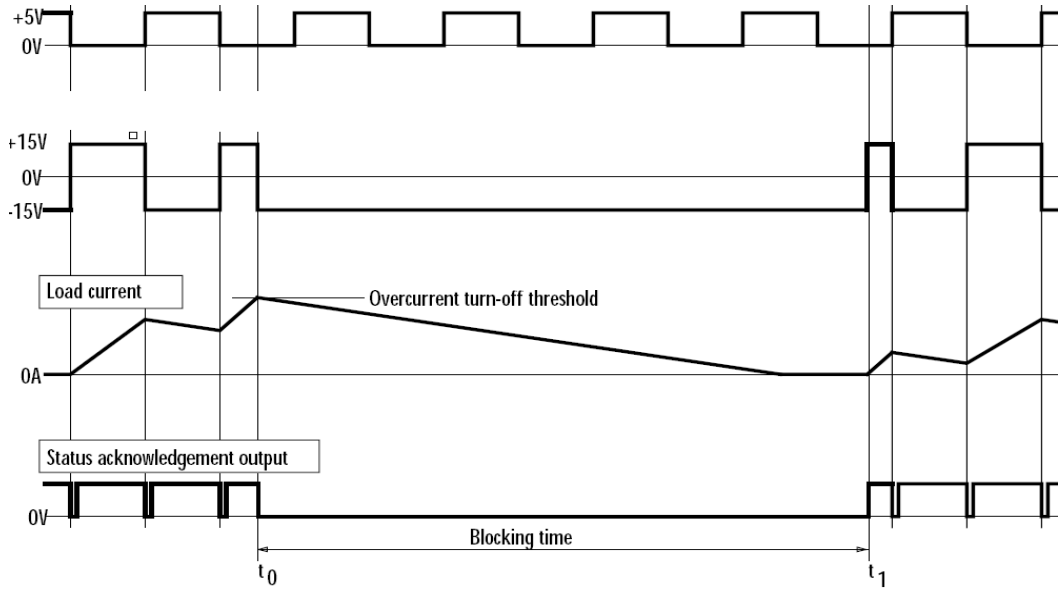
The acknowledgement function allows the control electronics to monitor the operation of both FOL connections as well as the driver.

If the acknowledgement pulse fails to appear, then the FOL drive

connection has probably failed. FOL connections that are incorrectly plugged in and transmit diodes whose luminous power is greatly reduced due to degradation effects often show the following extremely dangerous effect: the receiver emits a high frequency noise signal in the megahertz rang. This leads to thermal destruction of a power semiconductor and possibly also of the driver within short time. An acknowledgement pulse is then present at the SO output with every edge of the input signal. A defective status can be detected by a suitable logic circuit in the control electronics and the system can be turned off.

It is further recommended that the status acknowledgements are not connected together in the form of a summed message, ut are evaluated as individual signals in a monitoring logic circuit. This significantly simplifies diagnosis and troubleshooting in the event of a fault.

SO input logic and blocking time as below:



SO input logic and blocking time

Pin Cq

Acknowledgement Pulse Capacitor

After each module received a pulse successfully, it will feedback a pulse signal through SO.

The length of the acknowledgement pulse at the output SO is determined by a capacitor at this terminal connected to Pin COM. The length of this pulse can then be optimally determined for each application.

5.5 Notification

(1) The capacitor value between Pin 10 VDC & Pin 9 GND should be not less than the one between Pin 23 Cs and Pin 24 COM. And this capacitor value is less than 220uF.

(2) The connection wire should be less than 10 cm between IGD drive and power semiconductor. Twisted wire should be used for connection each power tube grid and Emitter electrode and measurement electrode (drain electrode, collector electrode).

(3) Try to reduce parasitic inductance of the circuit. The drive circuit and equalizer circuit are designed as printed plate in our modulator and assembled on the Pins of IGBTs directly, in this case to reduce the big counter potential phenomena caused by distributed inductance.

(4) Selected value for current-limiting resistance of fiber emitter terminal should be suitable. If the value is big, the fiber emitter current will be not enough, and this will affect the output pulse of the module.

6. Calculation of driving power

Gate input capacitance (Cin) can be found in the data sheet. The total power need to drive IGBT can be calculated by the following simple formula:

$$P=f*Cin*\triangle V^2 \quad OR \quad P=f*Q*\triangle V$$

$$\text{Gate charge } Q=\int idt=C*\triangle V$$

(Note: P stands for the real driving power not including the losses in drive channel and drive power supply.)

WEPOWER

WEPOWER TECHNOLOGY CO., LTD
NO. 2 YUEHE ROAD, XIXIANG TOWN,
BAO'AN DISTRICT, SHENZHEN,
CHINA 518102
TEL: +86-755-27796280
FAX: +86-755-27914685
Email: info@wepowertech.com
Http://www.wepowertech.com